Photonic Integrated Circuits for Access Networks

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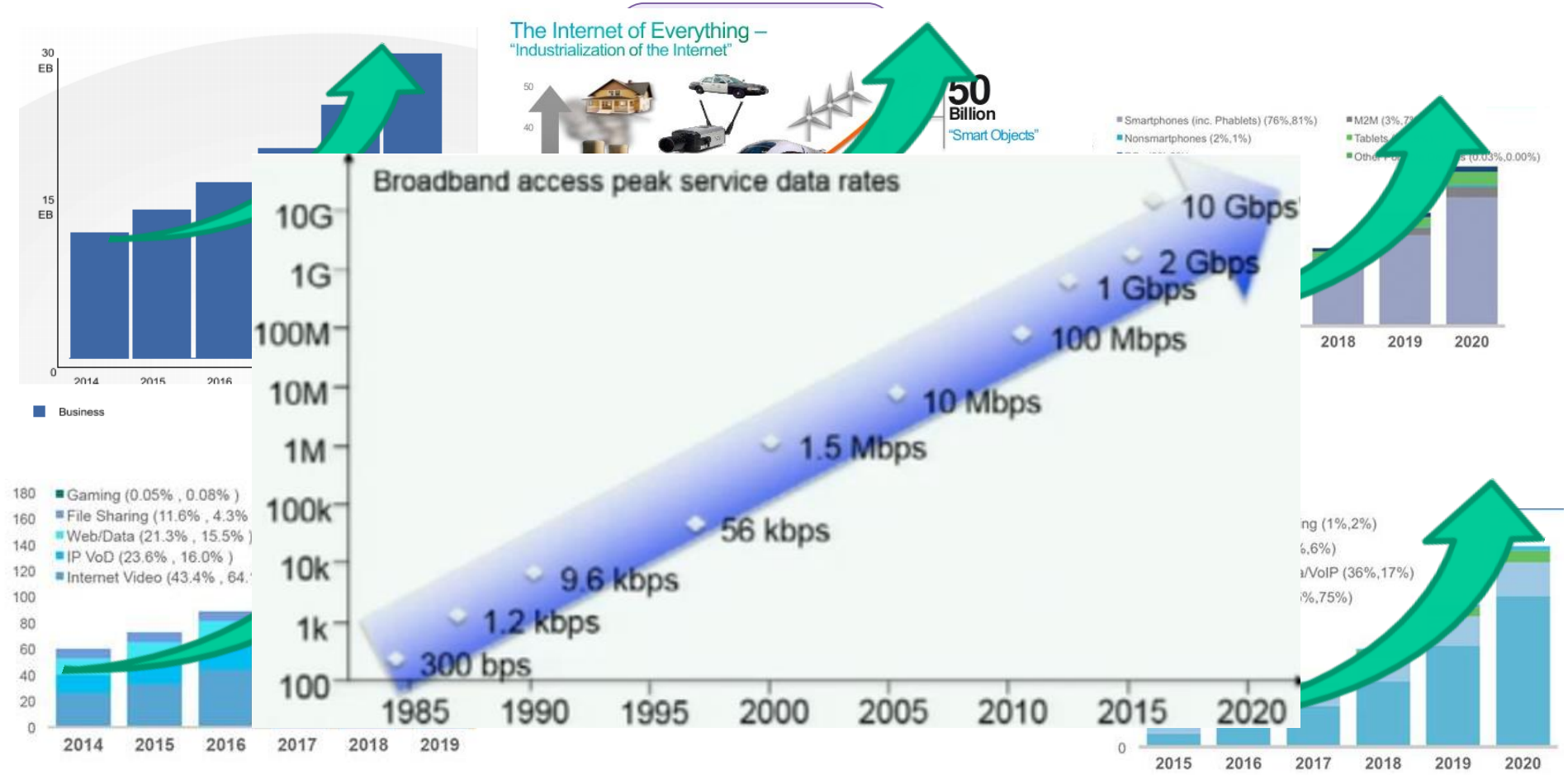
Demands on higher bandwidth are increasing

Access Capacity Motivation



C. Knittle, "IEEE 100 Gb/s EPON" OFC 2016.
Source : Cisco VNI

Context

Video enabler solution
- Best wavelength band, with small constrains

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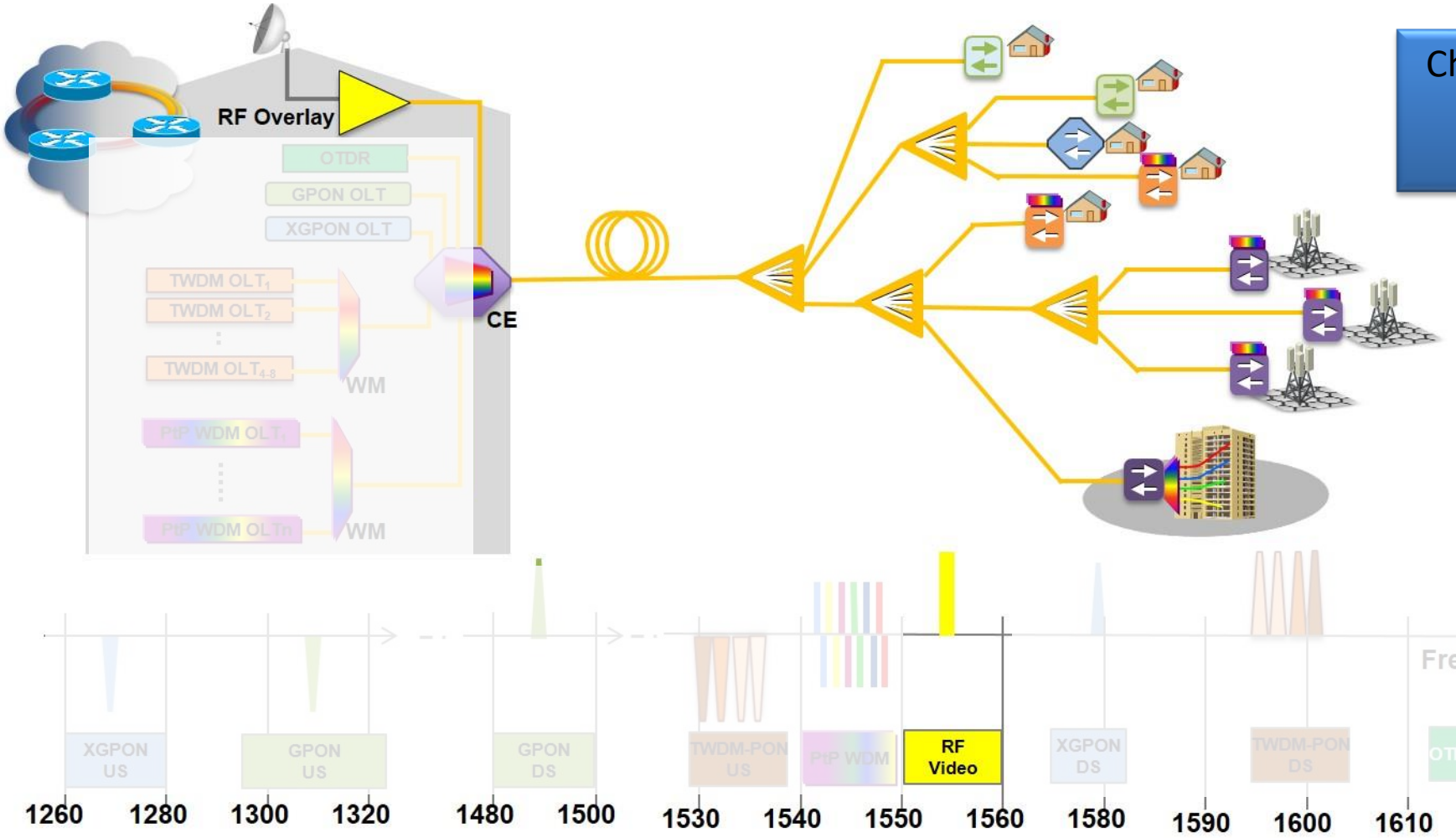
universidade de aveiro



Challenge: start fiber deployment/ adoption

Context

GPON solution
- Target low cost /reasonable bandwidth to compete with copper

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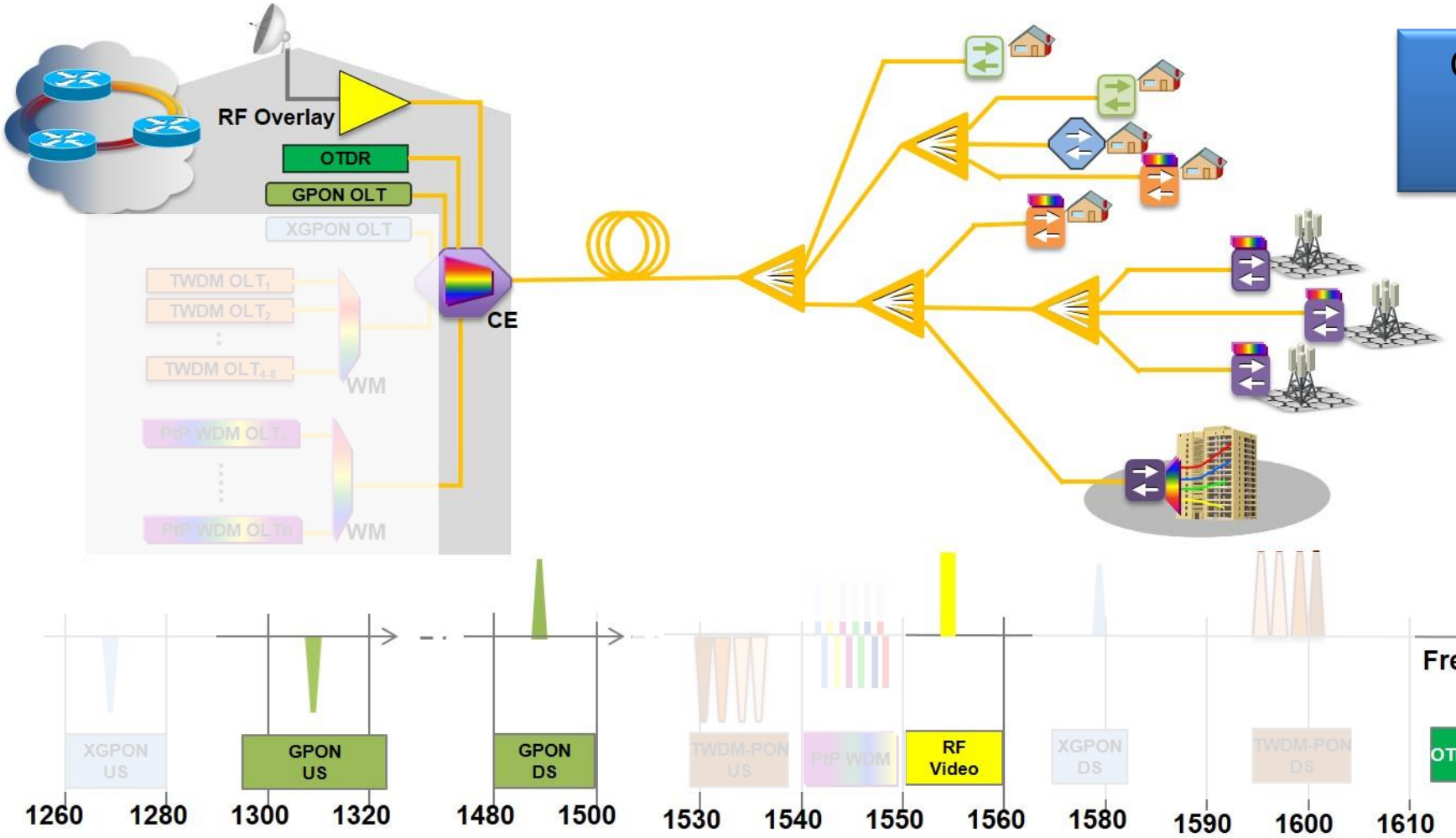

Challenge: get the volume to lower prices

Context

Trying to get further bandwidth with the same principles of GPON (US in low dispersion)

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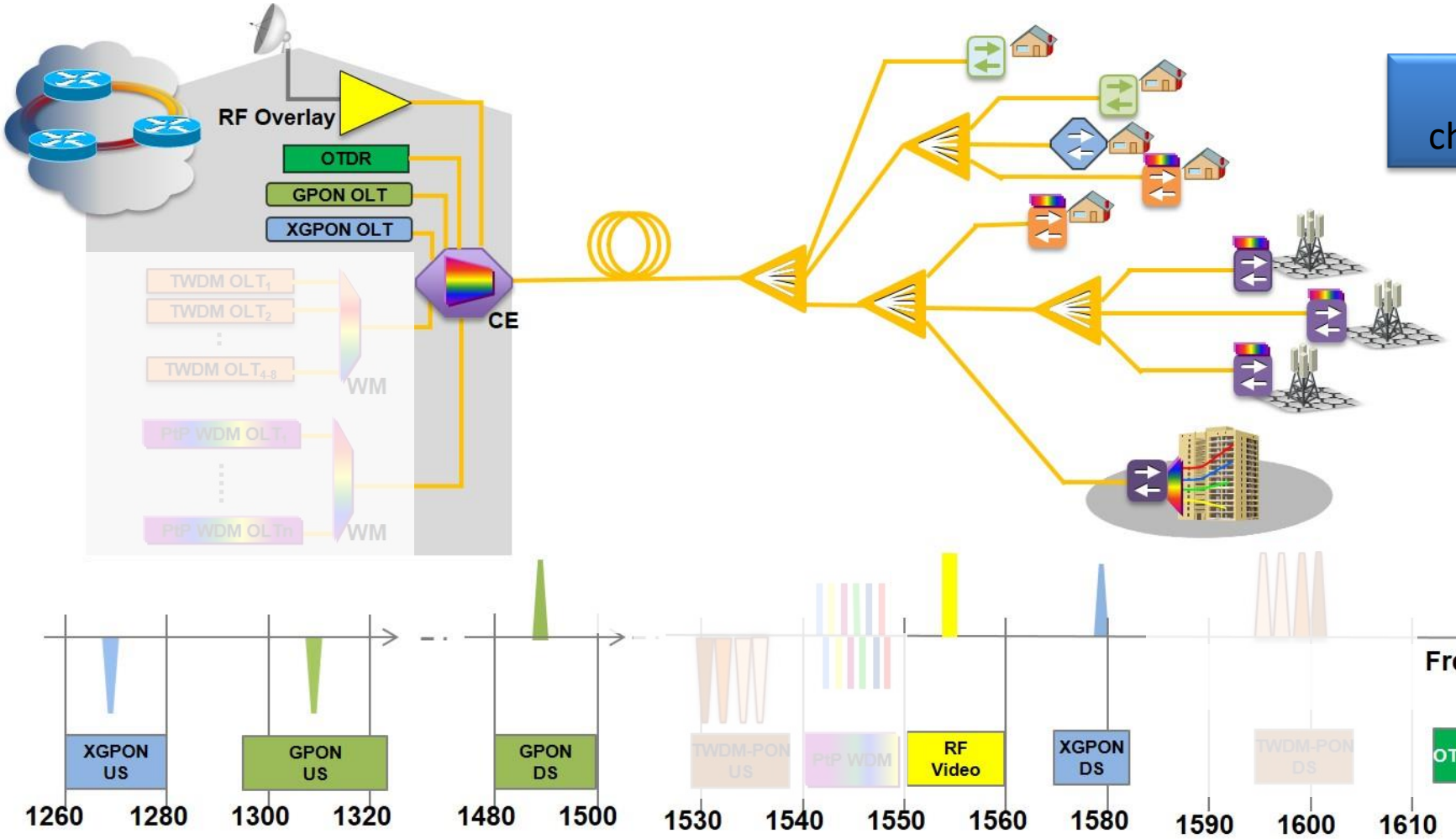

Context

Increasing substantially the bandwidth and adding flexibility

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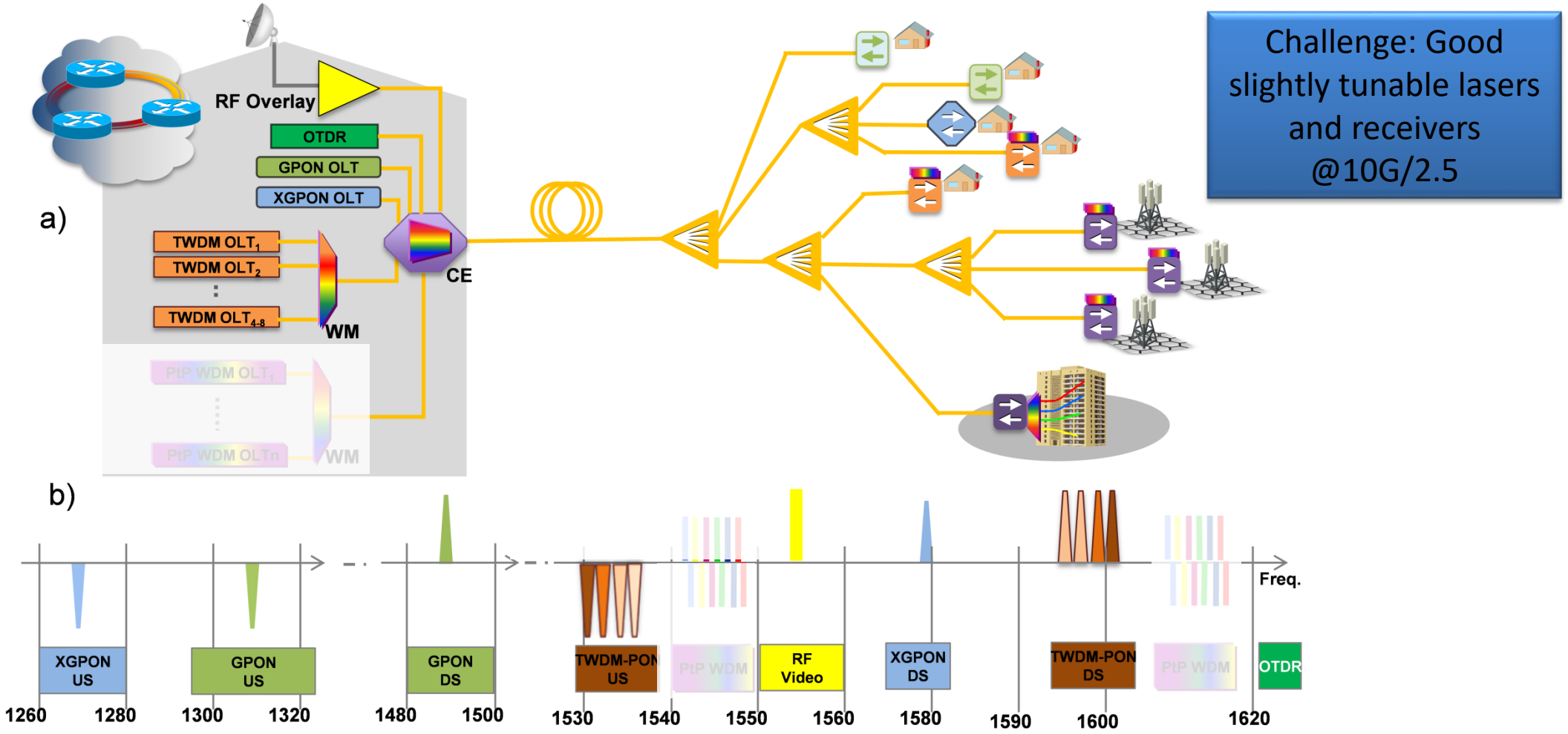

Challenge: Good slightly tunable lasers and receivers @10G/2.5

Context

Adding the extra flexibility and global control.

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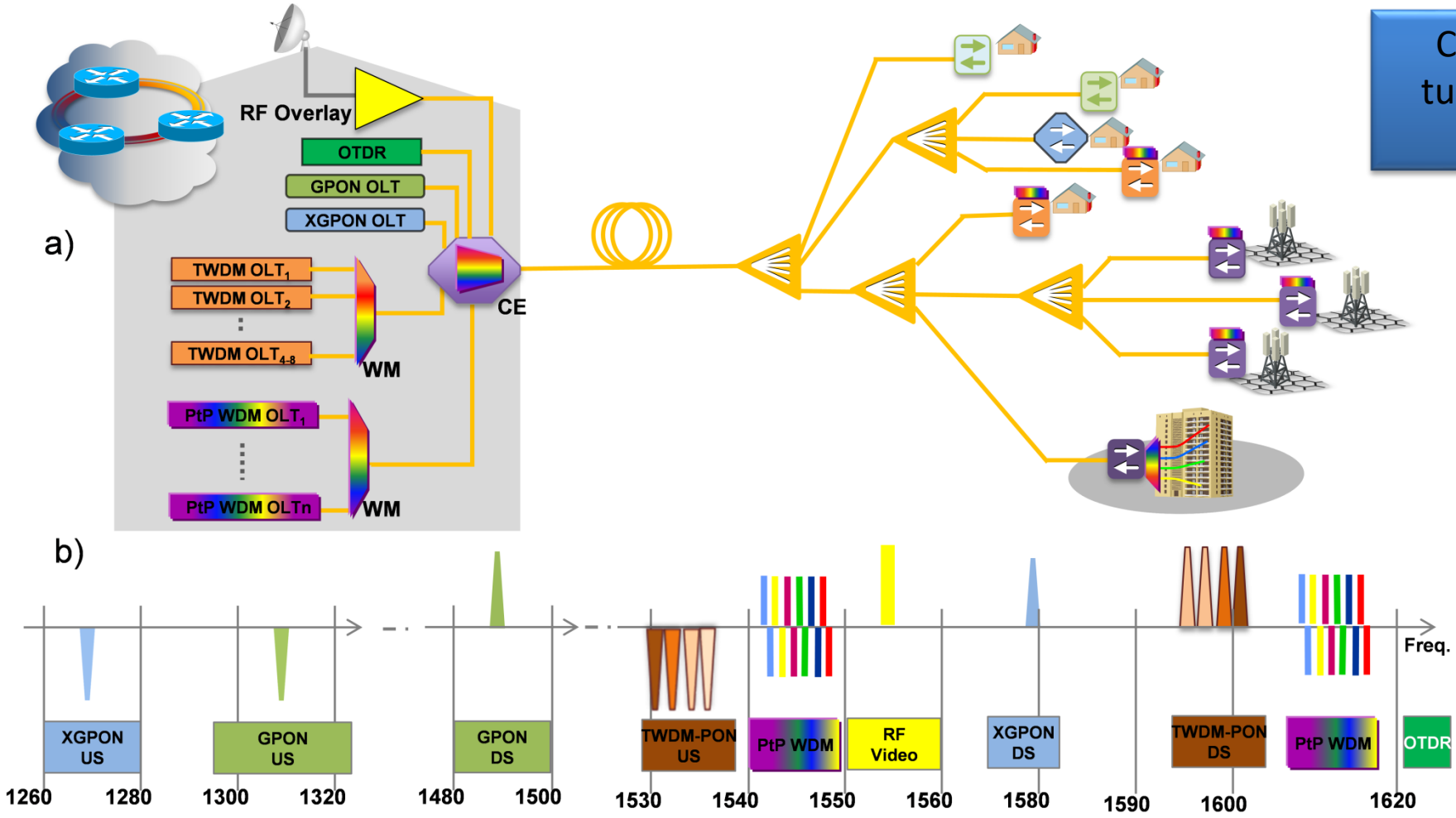
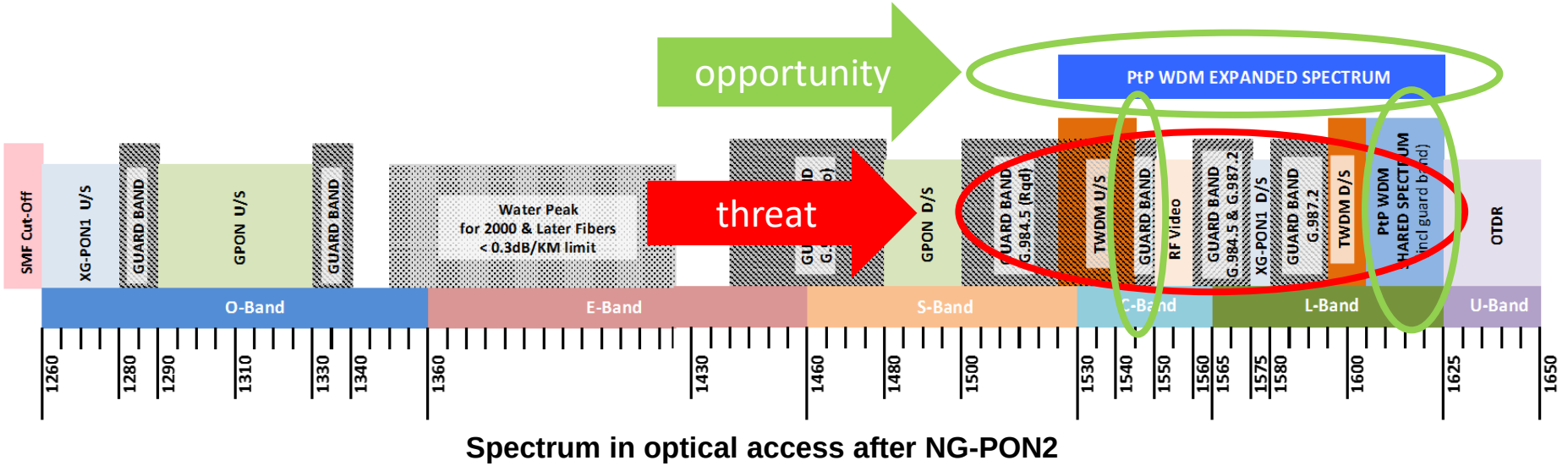
Challenge: Good tunable lasers and receivers



A. Shahpari et al, "Multiple System Configuration for Next Generation Optical Access Networks with Real-Time Nyquist UDWDM-PON", ECOC2015, P7.18

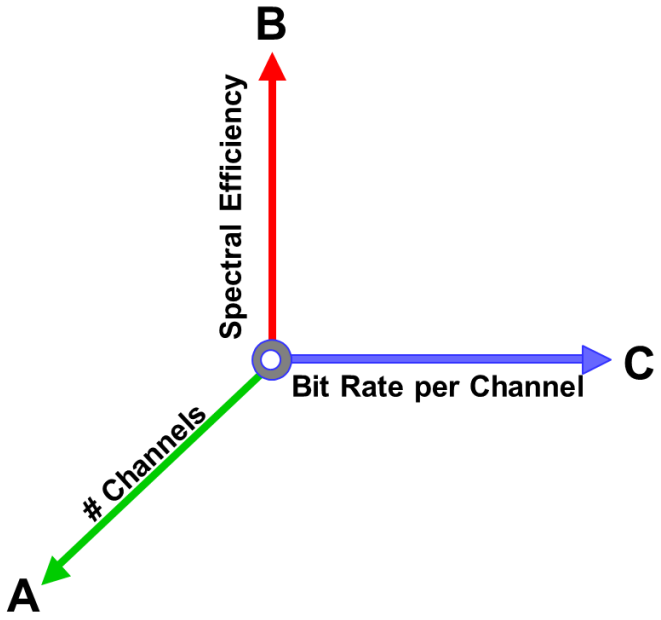
Context



Spectrum in optical access after NG-PON2

Future optical access networks will target:

- ❑ Higher data rate per user
- ❑ Spectral efficiency
- ❑ High number of user per ODN
- ❑ Extended reach
- ❑ Flexible network



ITU-T recommendation G.989.2 (draft), April 2014.

Current technologies

Essential (now)	Optional (near future)
Low Cost	Wide tunability
Slight tunability	High ODN loss tolerance
Tight control of wavelength	>10Gbit/s rate
10Gbit/s rate	High spectral density

GPON

NGPON2

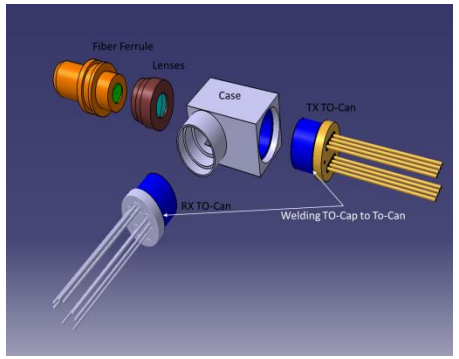
XGPON

DWDM+Coherent+

Advanced modulation formats

(Core+metro)

Current technologies – physical layer



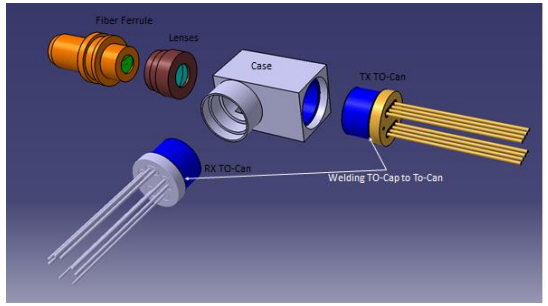
We have achieved:

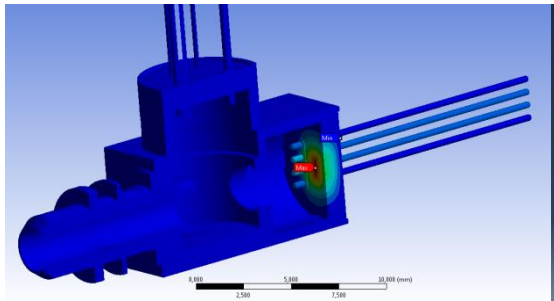
- Thermal capacity (packaging)
- Bandwidth (packaging)
- Combined optical performance (optical design)

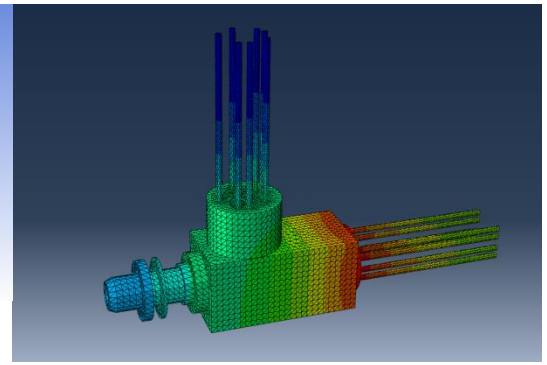
Simplification/Integration is needed

Tx:
Laser Diode
Lenses
TEC
Mirrors
Isolators
Beam splitters
...

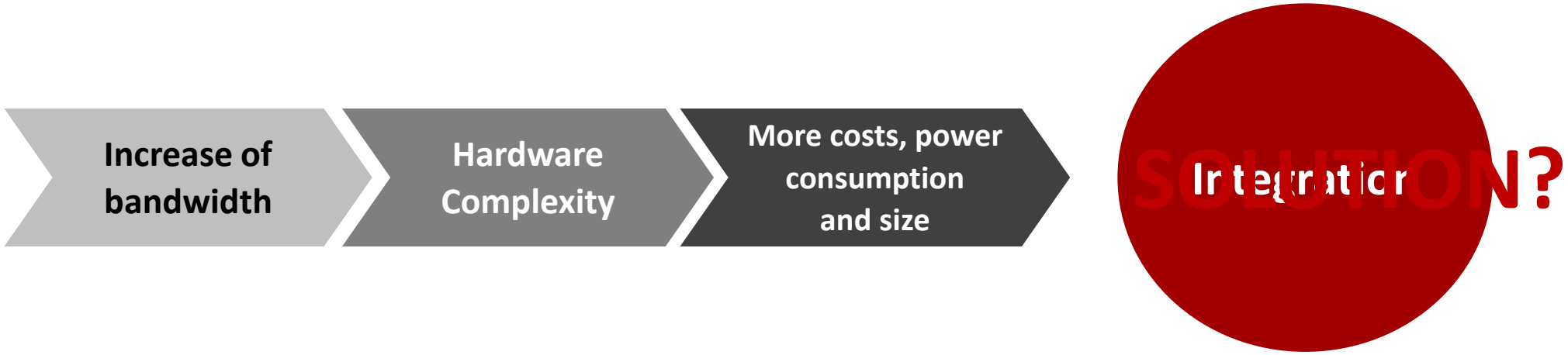
Rx:
Photodiode
Lenses
Mirror
Thermistors
...







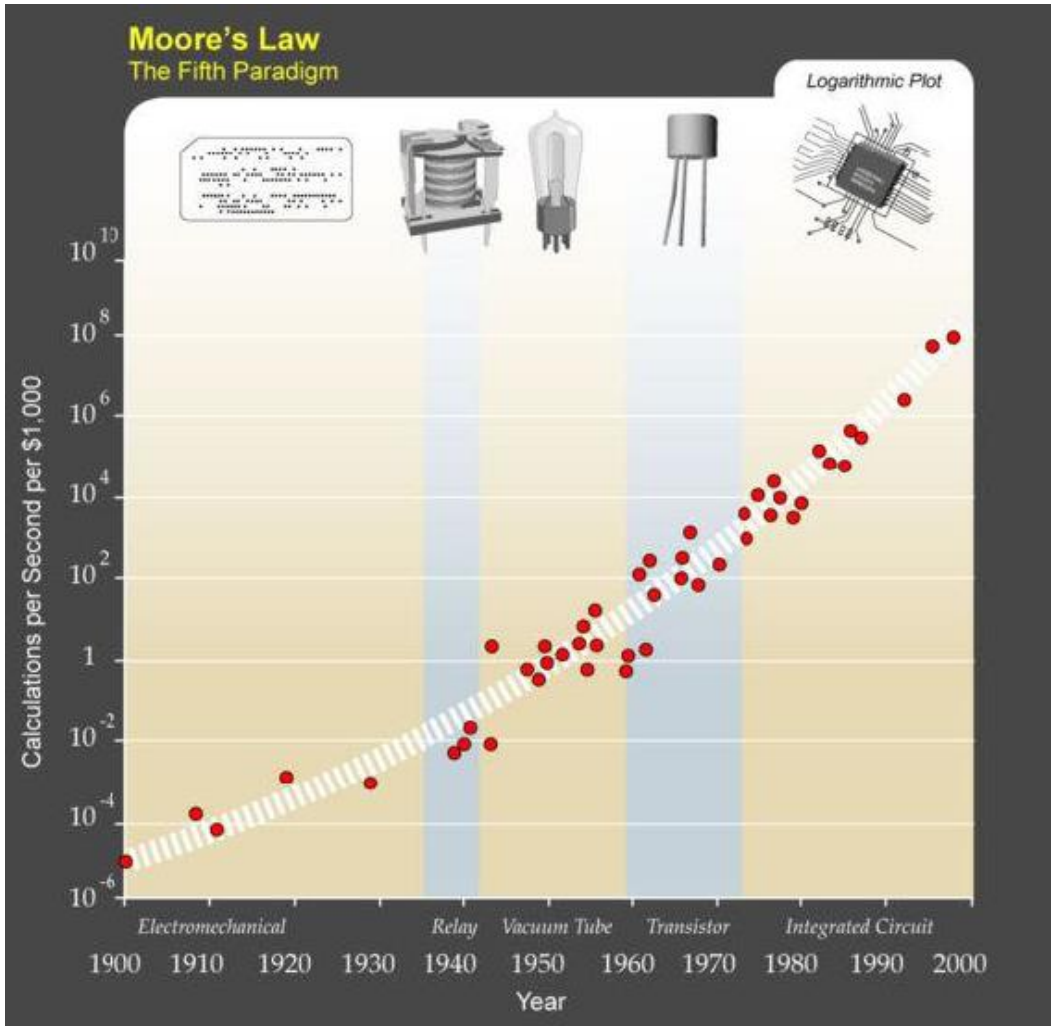
How to follow the increase of bandwidth in the devices level?



Integration was crucial in *electronics*

In the integration world

In electronics we are governed by Moore's Law



Source: Infinera

Integration brought:

- More functions
- Less space
- Less power consumption
- Mass deployment of technology to everyone at a lower cost

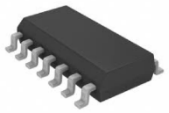
In the integration world

Electronics

Vacuum tubes

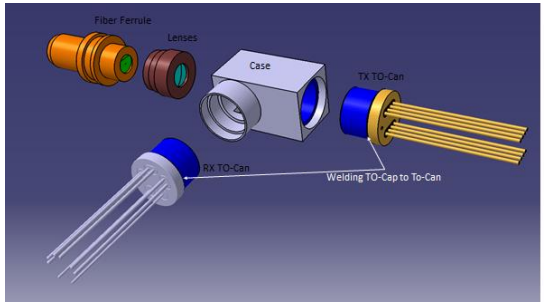
Transistor

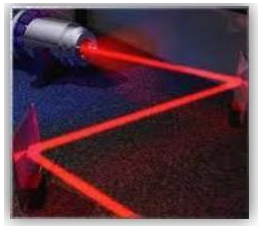
ICs



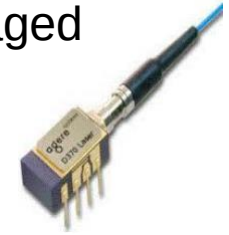
Optics

Free space components

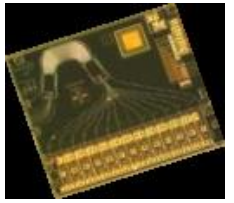


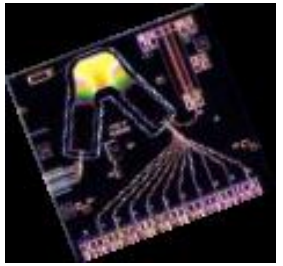


Single components packaged

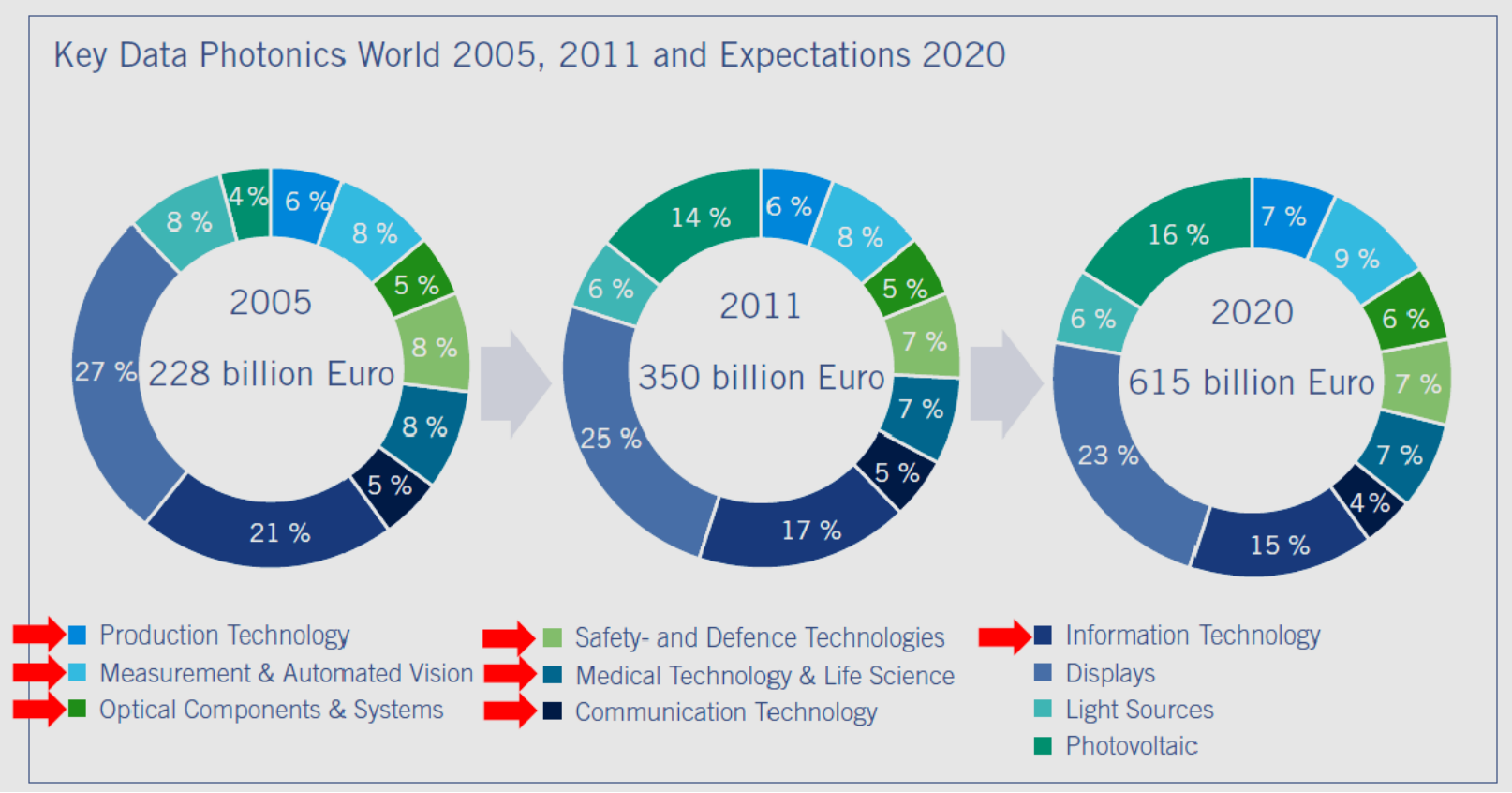


PICs





The Photonic Market



Source: COBRA

Markets and applications

Large markets (low-cost and high volumes)

- Datacom
- Telecom access

High added value (medium and low volume)

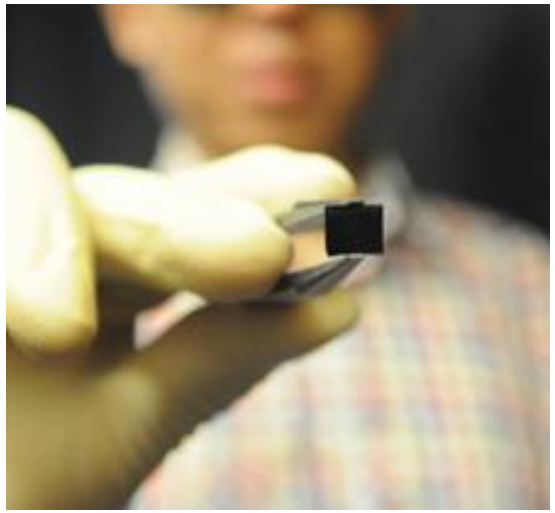
- Telecom high end
- Medical diagnostics
- Sensors redouts
- Metrology

In our research group we are focused to develop PICs for telecommunication purposes

Why PICs?

Increased bandwidth

Increased hardware complexity and control



http://www.photonics.com/images/Web/Articles/2010/11/1/Figure1_2.jpg

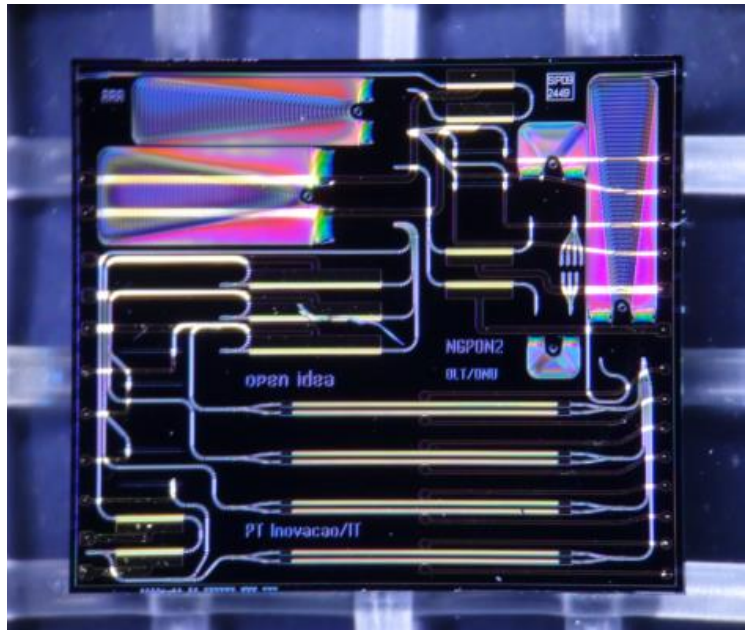
Increase costs, power consumption, floor space

- From investment and realization point of view can become unbearable to keep with discrete components.

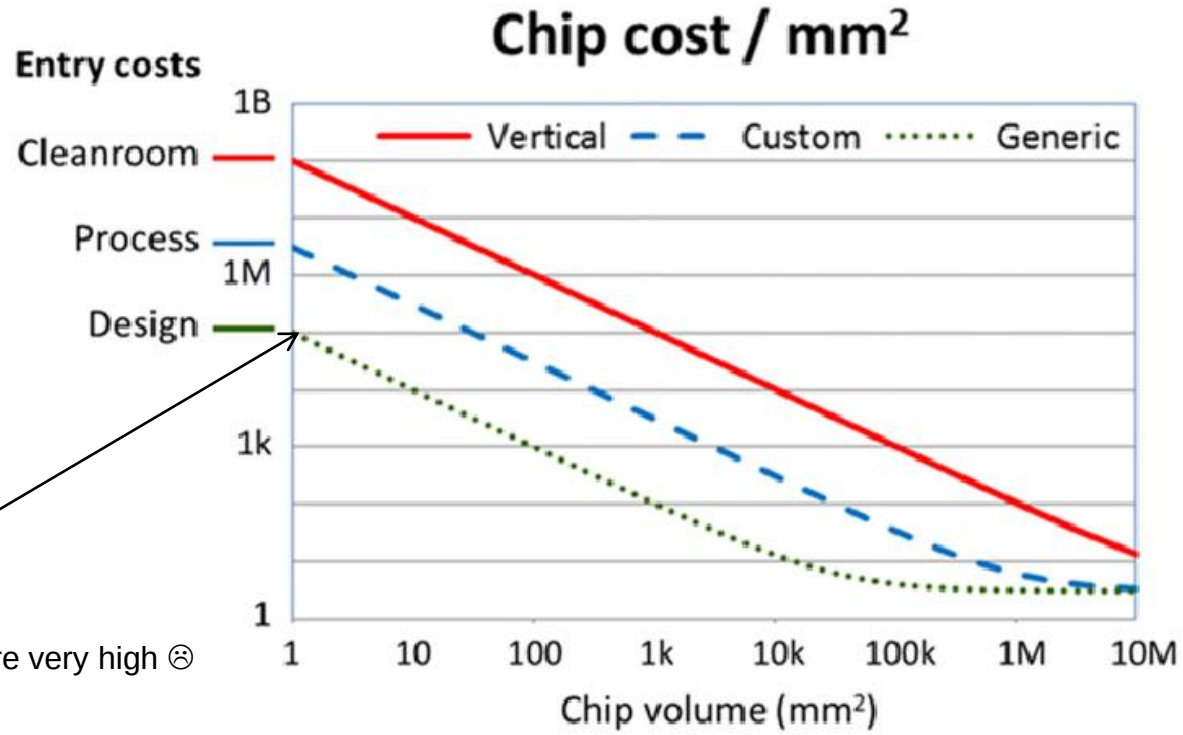
Why PICs?

> ***PICs are the way to make the systems and subsystems ubiquitous***
> – M Smit

+ Integration in a single chip
  - Lasers
  - Modulators
  - Amplifiers
  - Detectors
+ Decrease size and power consumption
+ Improves reliability
+ Reduce the O-E-O conversions



PICs what are the R&D costs?

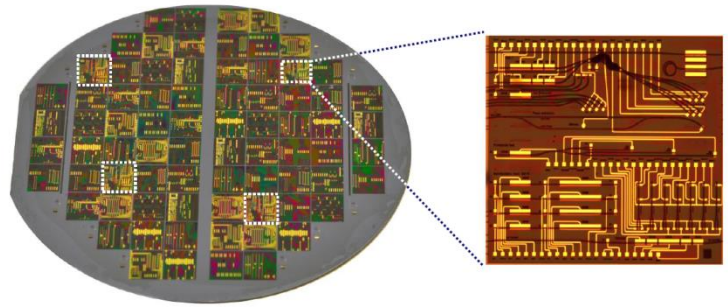


Source: doi:10.1049/iet-opt.2010.0068

At low chip volume (R&D) the prices are very high ☹

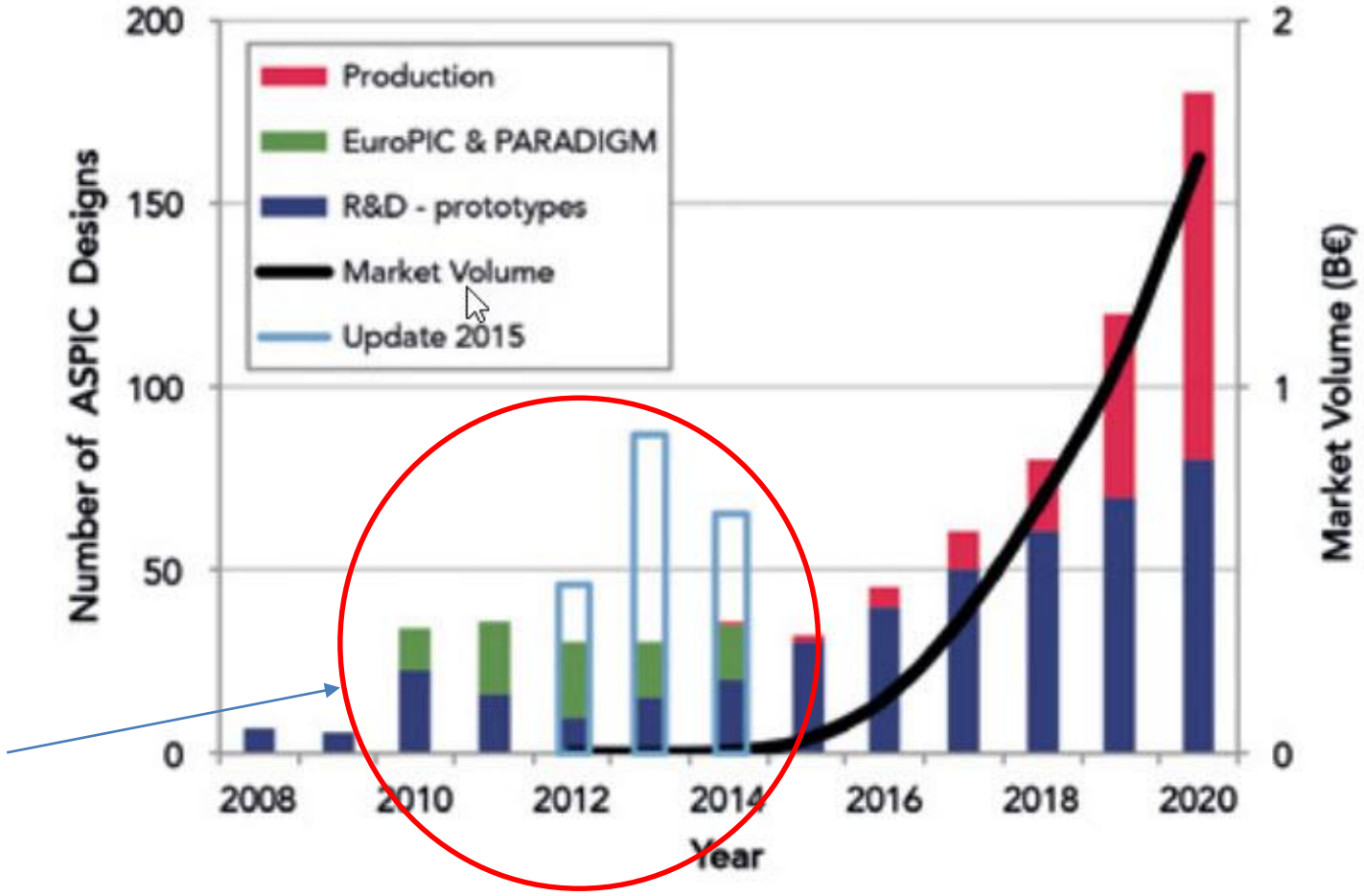
Solution: **Multi Project Wafer Runs**

Cost sharing in R&D phase



Source: COBRA

Adoption and Market volume



Early adoption by funded projects

Source: JEPPIX Roadmap

Simple building blocks …. All combinations are possible

Passive devices are available in all platforms

- MMI couplers, filters and reflectors
- AWG-demux
- Ring filters
- Polarisation splitters and combiners

....

Switches and modulators are available only in InP and Silicon

- Phase modulator
- Amplitude modulator
- Fast space switch
- WDM crossconnect, WDM add-drop

....

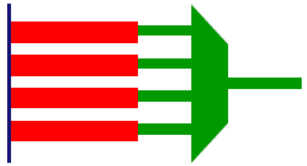
All kind of lasers and amplifiers (only in InP)

- Fabry-Perot lasers

- Tunable DBRs

- Multi wavelength lasers

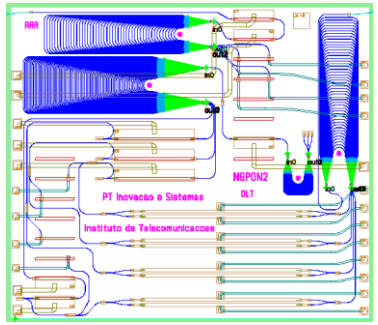
....



Source: COBRA

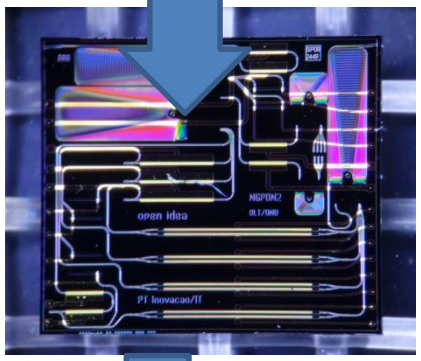
InP is the most suited platform for developing Telco subsystems ☺

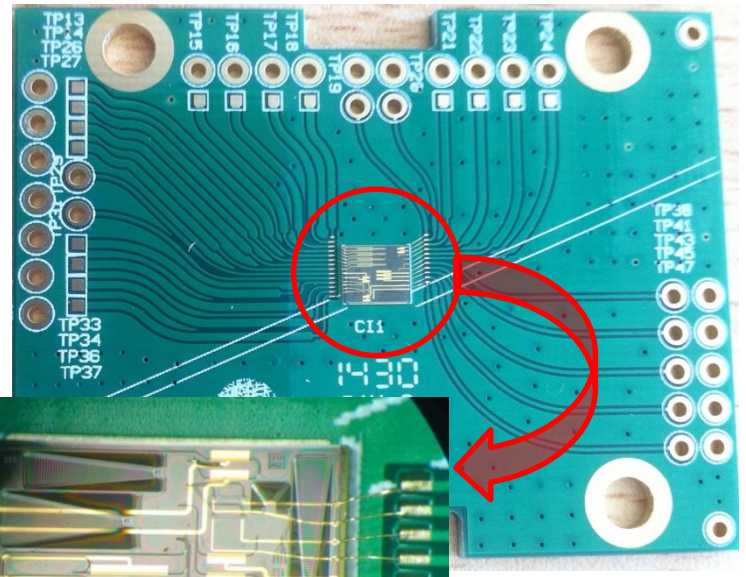
How we do it: Full process control



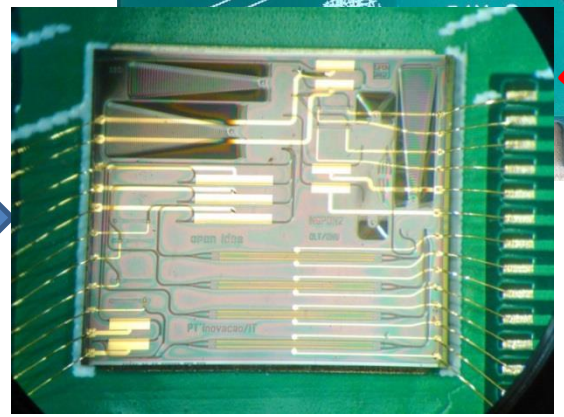
Design

Production





Packaging



Our first focus was **design** however now we are *also focused* on the **packaging** with a lot of scientific and technical problems to overcome

Process flow

Project Definition	PIC Design	Fabrication	Testing
+ Choose the type of integration – Monolithic integration – Hybrid integration + Choose the subtract material – InP – Silicon – TriPlex	+ Simulate the components/circuit + Proof of concept + Layout design + Mask Generator	+ MPW runs	+ Electrical and optical tests + Packaging

MPW runs – generic foundry service

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InP based photonics	TriPleX™ photonics (SiO_2 / Si_3N_4)	Silicon photonics
JePPIX	LioniX	ePIXfab
• SmartPhotonics (TU/e, COBRA); • FhG/HHI; • Oclaro	• TriPleX™	• CEA-Leti; • IMEC; • IHP

+ Project Definition

Technologies and Foundries

InP based photonics

- SmartPhotonics
- HHI;
- Oclaro

TriPleX™ photonics (SiO_2 / Si_3N_4)

- TriPleX™

Silicon photonics

- imec
- IHP
- LETI

	Performance		
Building block	InP	Si	TriPleX
Passive components	●	●	●
Lasers	●●●	○	○
Modulators	●●●	●●	●
Switches	●●●	●●●	●
Optical amplifiers	●●●	○	○
Detectors	●●●	●●●	○

Footprint	●●	●●●	●
Chip cost [1]	●	●●	●●
CMOS compatibiity	○○	●●	●
Low cost packaging	○	○[2] / ●●[3]	●●

Performance	
●●●	Very good
●●	Good
●	Modest
○	Challenging

1 Cost also depends on volumes.
Refer to the JePPIX cost roadmap.

2 Endfire coupling : broadband,
low reflection and polarization insensitive

3 Vertical coupling: exploits surface
coupled grating technology

+ Project Definition

Technologies and Foundries

Broker	Process	Lasers	SOAs	TBR	Modulators / Phase shifters				Detectors			Prop loss	MPW cost			
					L (mm)	Vp - Pp	Loss (dB)	B (GHz)	R(A/W)	B (GHz)	Idark (nA)	dB/cm	Smallest chip	Price	MPW cost/mm²	#chips
JePPIX	Oclaro TxRx 10	YES	YES	YES	1	3,5	< 2	> 10	0,8	10		2-3	2 x 6	€ 12.000	1000	8
JePPIX	HHI Rx 40				0,5	(25 mW)	< 2	(kHz)	0,8	40	< 10	1-2	3 x 6	€ 5.500	300	8
JePPIX	SMART TxRx10	YES	YES		2	7	< 2	10	0,8	10	< 20	3-4	2 x 4.6	€ 4.500	500	8
JePPIX	TriPleX (DS-500-170)				1-2	(500 mW)	< 0.1	(kHz)				< 0.5	16 x 16	€ 16,000[1]	63	4
ePIXfab	imec ISIPP25G				1,5	8,5	5	11	0,5	> 50	< 50	1.5-2.5	2.5 x 2.5	€ 10.000	1600	10
ePIXfab	CEA-LETI Full Platform				1-4.7	?	?	10	?	10	?	?	3.4 x 3.7	€ 21.750	1700	50
OPSiS[2]	OpSIS-IME OI50				3	9	5	30	0,7	> 50	3300	1-2	2.5 x 2.5	€ 8.000	1300	20

Footnotes: [1] universities get 45% reduction on TriPleX MPWs, [2] OPSIS stopped brokering service in 2014

Table 1 Comparison of the most important features of MPW-service for different platforms in 2014.

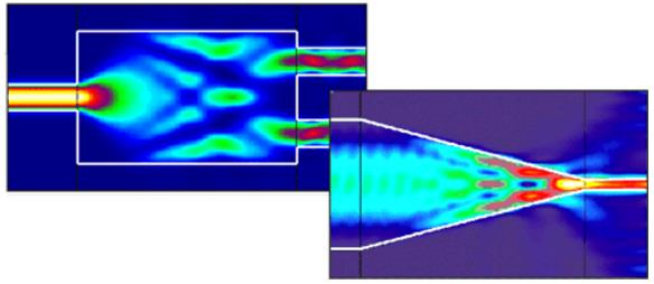
Design

• Aspic	• OptoDesigner • FieldDesigner • MaskEngineer • FlowDesigner	• CleWin 5	• Klayout

+ PIC Design & Simulation

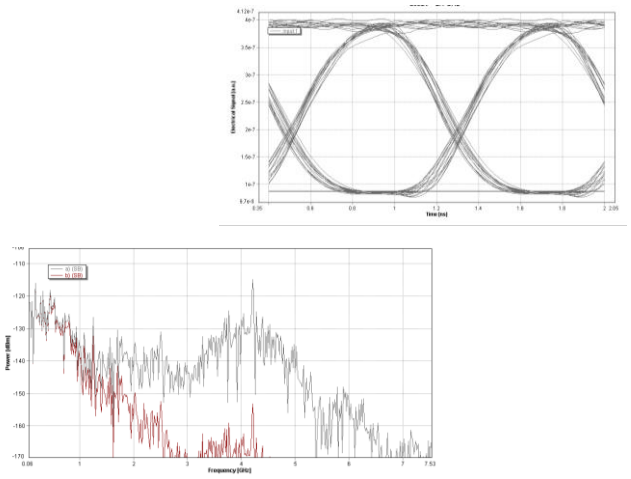
Photon Design

- Simulate propagation in waveguides
- Tool for both active and passive designs
- Include PDK for HHI and Smart Photonics



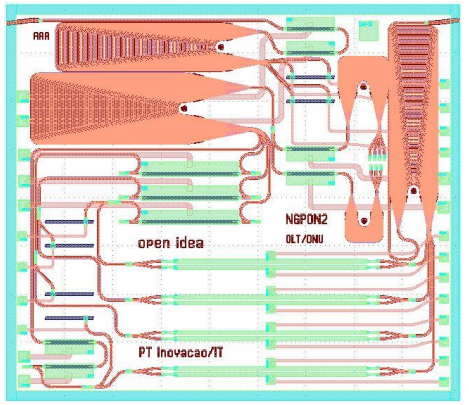
VPIphotonics

- Simulation software
- Capable of design, analyze and optimize components



Phoenix Software

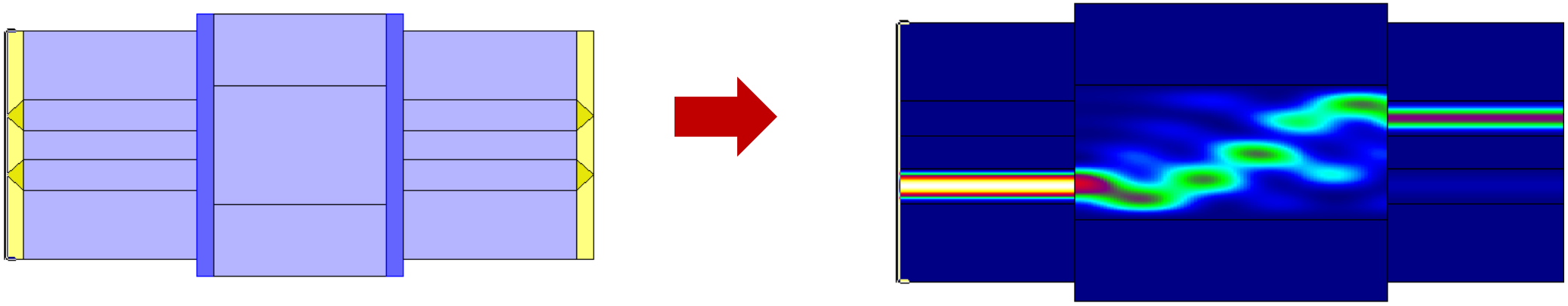
- OptoDesigner
- Supports MPW services
- MaskEngineer



+ PIC Design & Simulation

FIMMWAVE & FIMMPROP

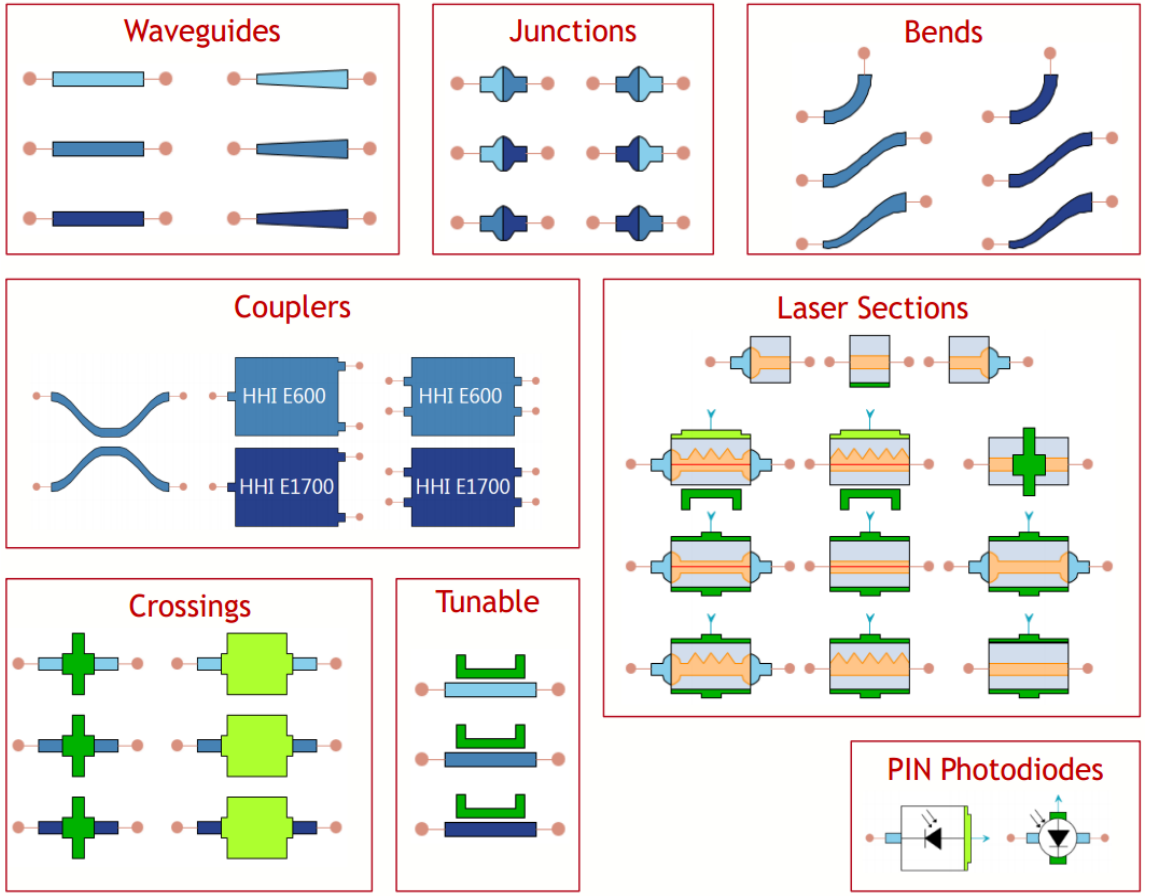
- From PhotonDesign
- Simulate propagation in optical waveguides
- Tool for optimisation of devices such as MMI Couplers
- Modelling optical structures
- Electromagnetic field using:
  - BPM
  - FEM
  - FDTD



+ PIC Design & Simulation

VPIphotonics ™ PDK HHI

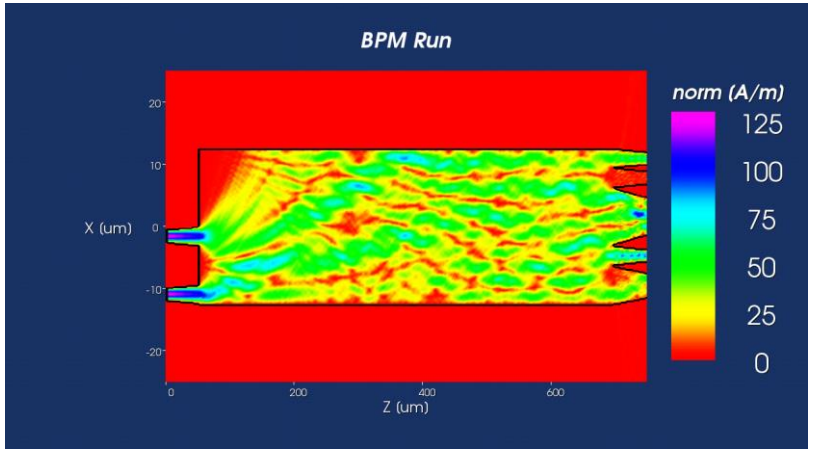
- Supports InP-based monolithically integrated photonic circuits offered by **Fraunhofer HHI**;
- It covers most of the building blocks (BB) from HHI;
- It allows to design a prototype for a PIC;
- Automatically export the circuit to OptoDesigner software;

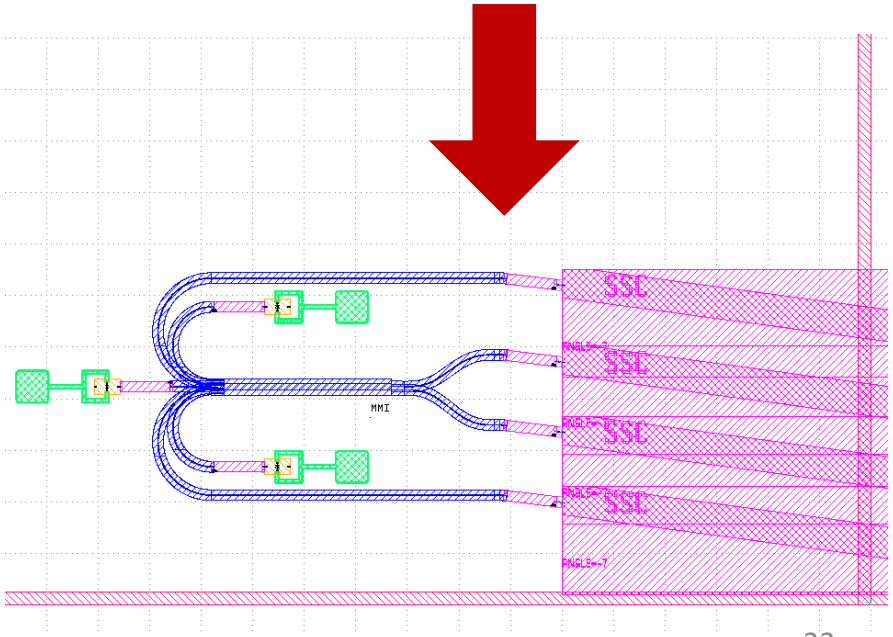


+ PIC Design & Simulation

Optodesigner

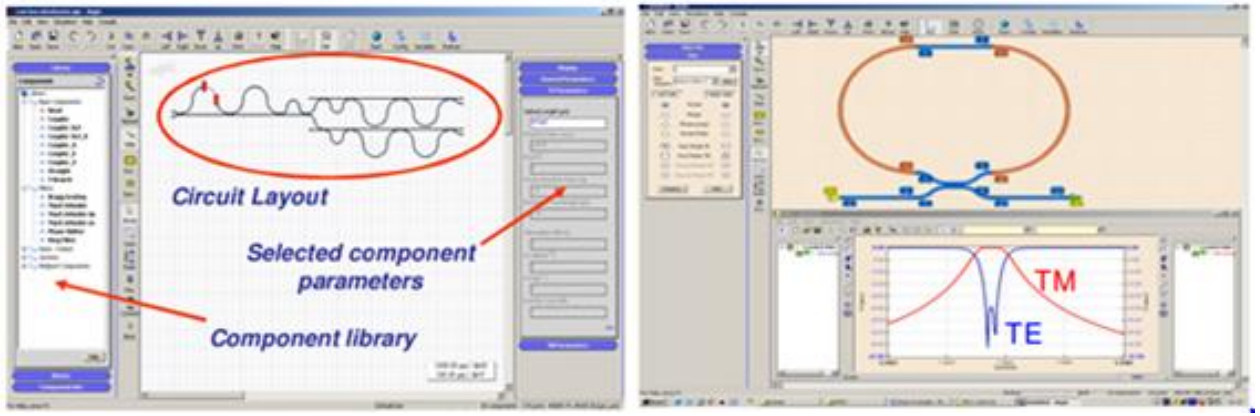
- From PhoeniX software
- Electromagnetic field using:
  - BPM
  - BEP/EME
  - FDTD
- Use of scripts for design and simulation
- Design rule checking





Design:Aspic

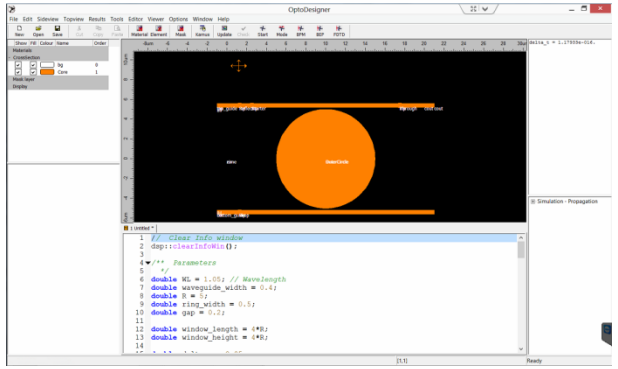
- Frequency domain circuit simulation (TE e TM):
  - Intensity;
  - Phase;
  - Group delay;
  - Disperson.
- Drag & drop interface;
- Export simple circuits to Mask Engineer;
- Export results for .mat ou .txt for post-processing;

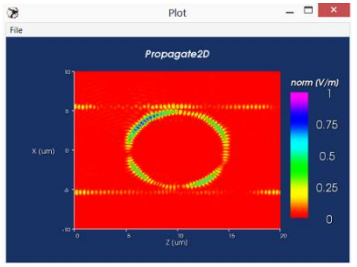


Source: Phoenix

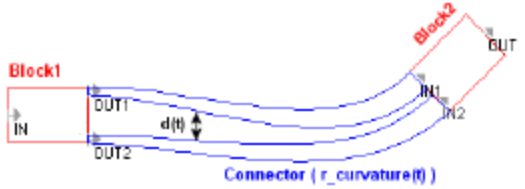
Design:OptoDesigner

- Electromagnectic field field simulations:
  - BPM (Beam Propagation Method);
  - BEP/EME (Bidirectional Eigenmode Propagation);
  - FDTD (Finite Difference Time Domain).
- Script based simulations and circuit design with elastic connectors;
- Simulation from waveguide cross section to top view propagation;
- Photonic Design Kits from different foundries
- *Design Rule Checking*;
- Export mask to well known .gds files
- Export results for .mat ou .txt for post-processing;



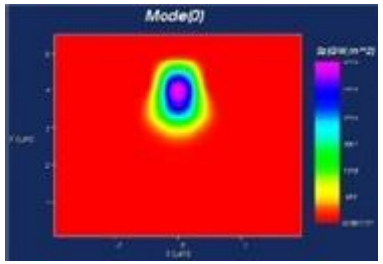


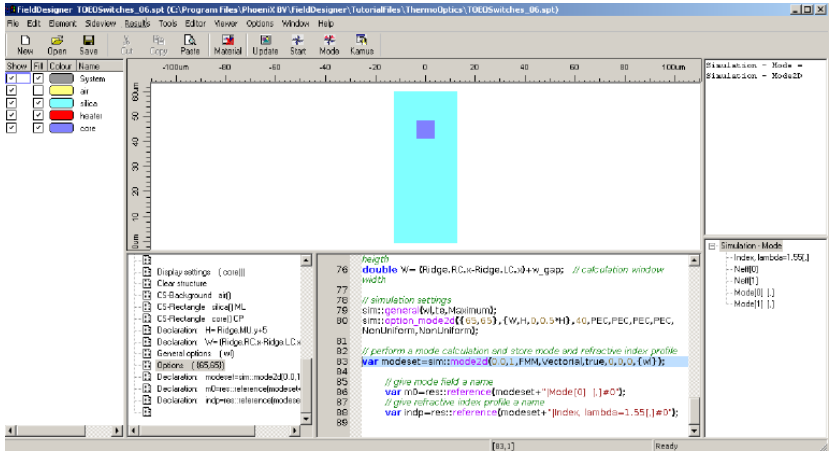
Source: Phoenix



Design:Field Designer

- Propagation of TE e TM (mode solvers):
  - FMM (Field Mode Matching);
  - FD (Finite Difference).
- Script based simulation setup ;
- Cross section view;
- Export results in .mat, .txt ou .xls for post-processing;



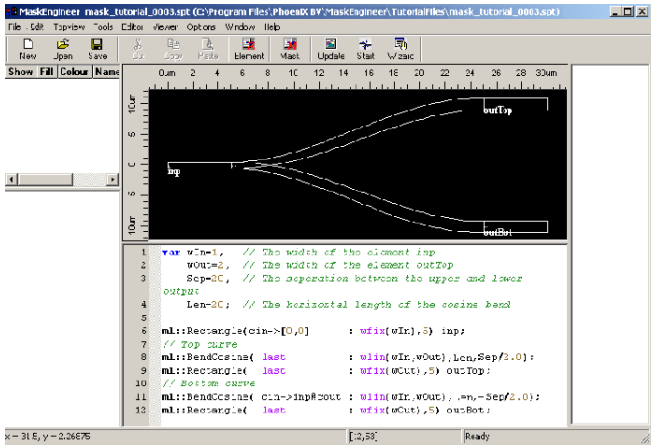


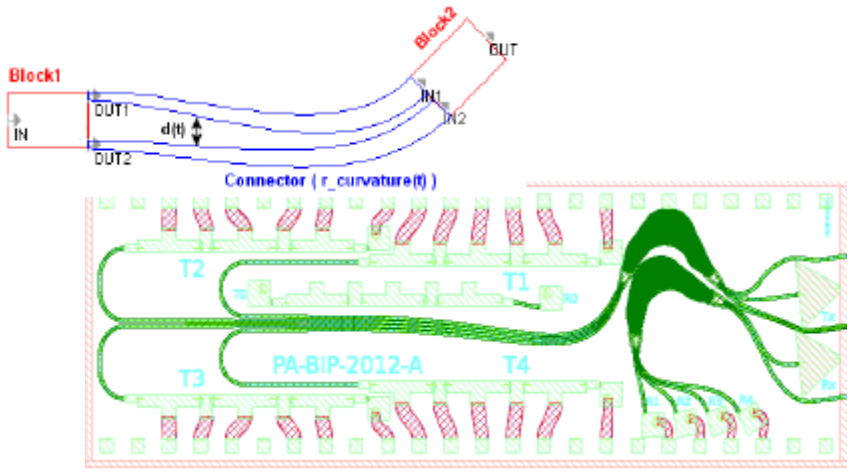
Source: Phoenix

Design:Mask Engineer

- Design of full circuit mask:
  - Possbility to develop own building blocks or use photonic design kits from foundries;
  - Absolute or relative position of the elements = elastic connection;
- Script based design with dialog-box interface;
- Export mask to well known .gds files
- *Design Rule Checking*;

Source: Phoenix

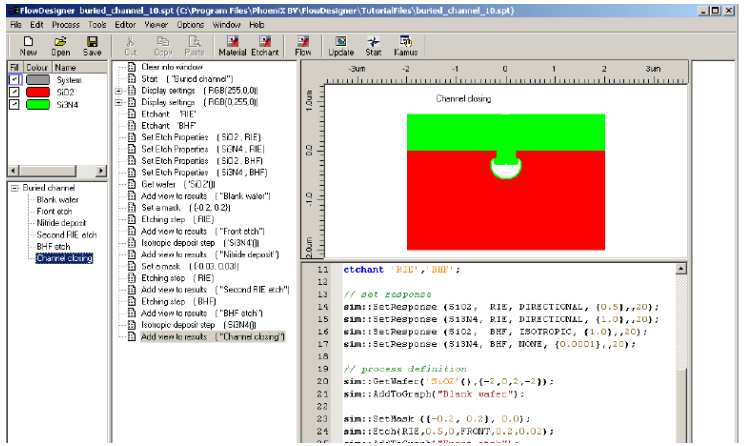


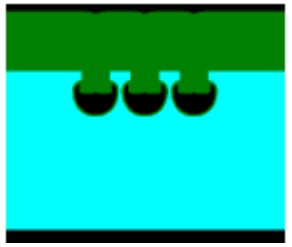


Design:Flow Designer

- Most indicated for foundries but good tool to understand foundry constraints;
- Cross section view of the stack;
- Script based process definition;
- Problems from the fabrication can be mitigated (e.g. Underetching, impurity) or try new material layers for specific purposes

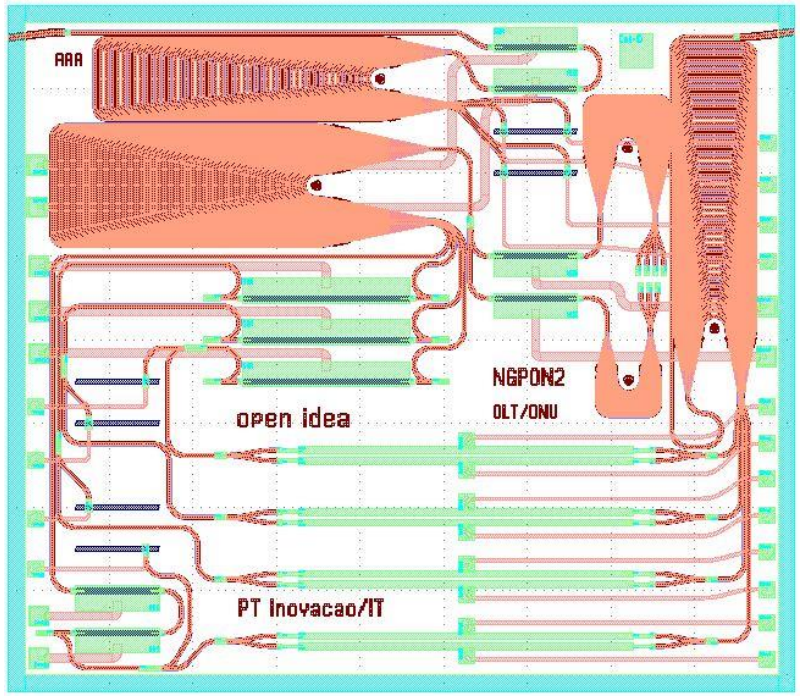
Source: Phoenix



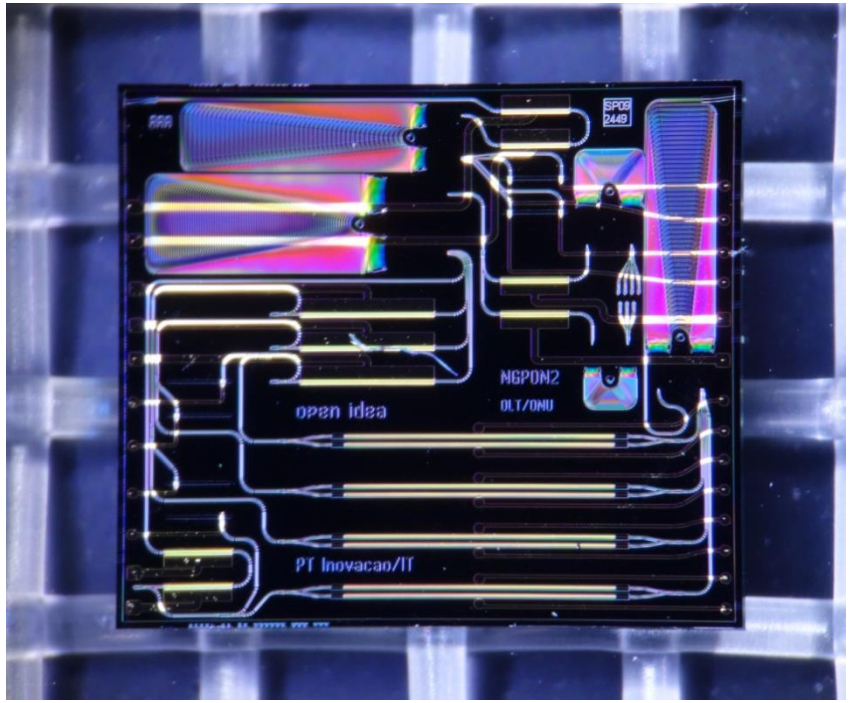


Production

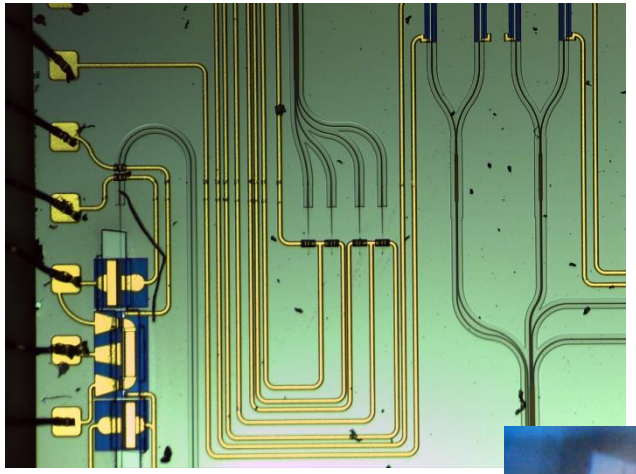
Final mask

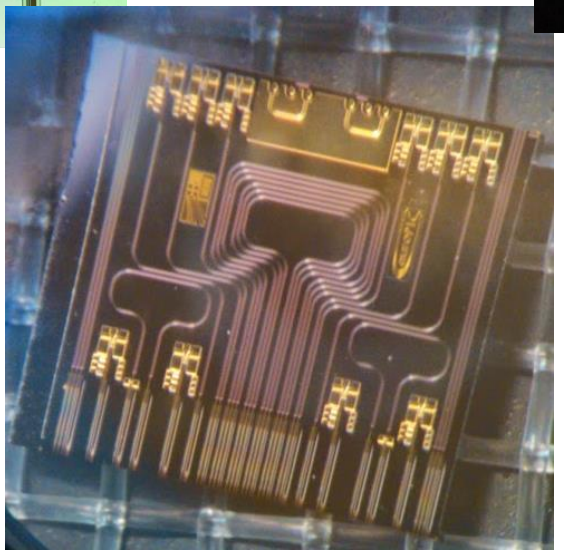


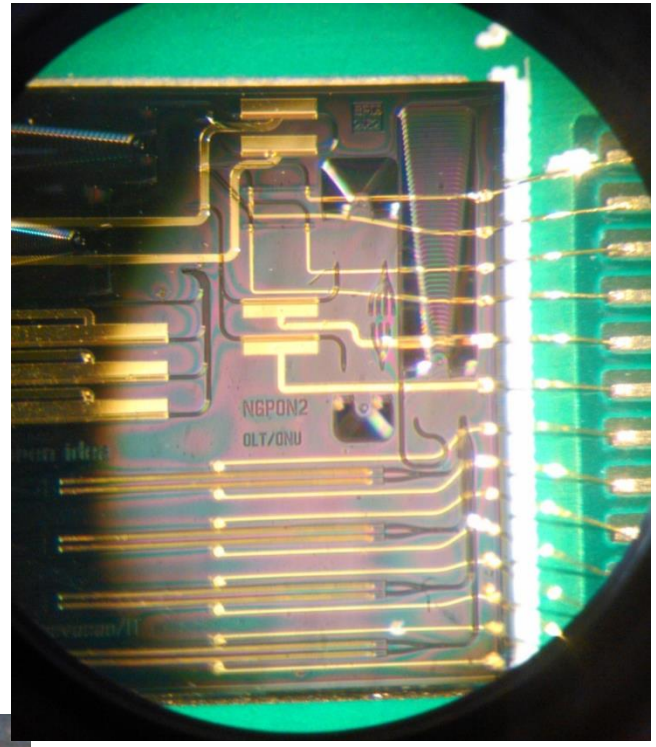
Chip received

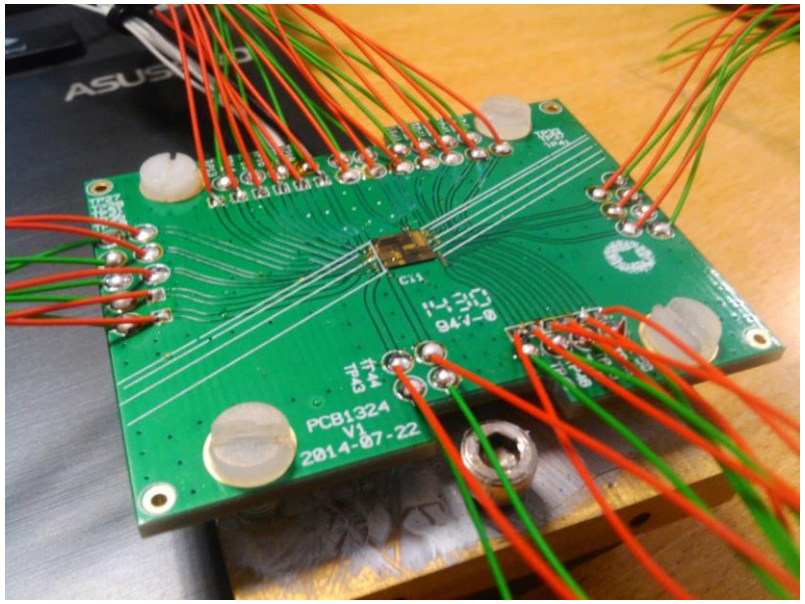


+ Fabrication









EXAMPLE OF DEVELOPMENT PHASES

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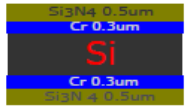
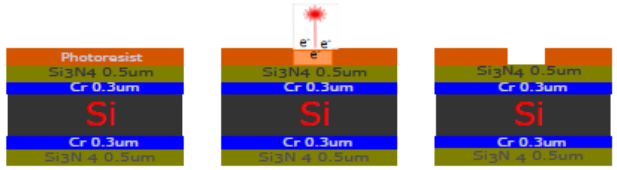
Etching Process and Fabrication

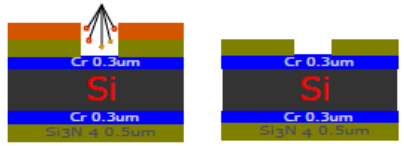
1. Deposition of Hard Mask Materials



2. Photoresist Deposition + Lithography + Pattern Develop

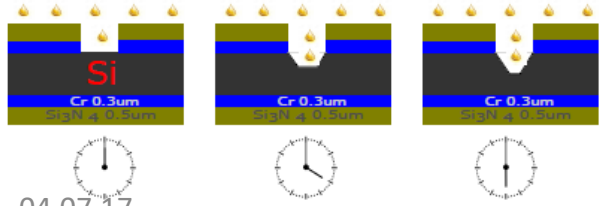


3. Etch Si_3N_4 (Reactive Ion Etching) and Photoresist Removal



4. Cr Wet Etching - Chemical Bath

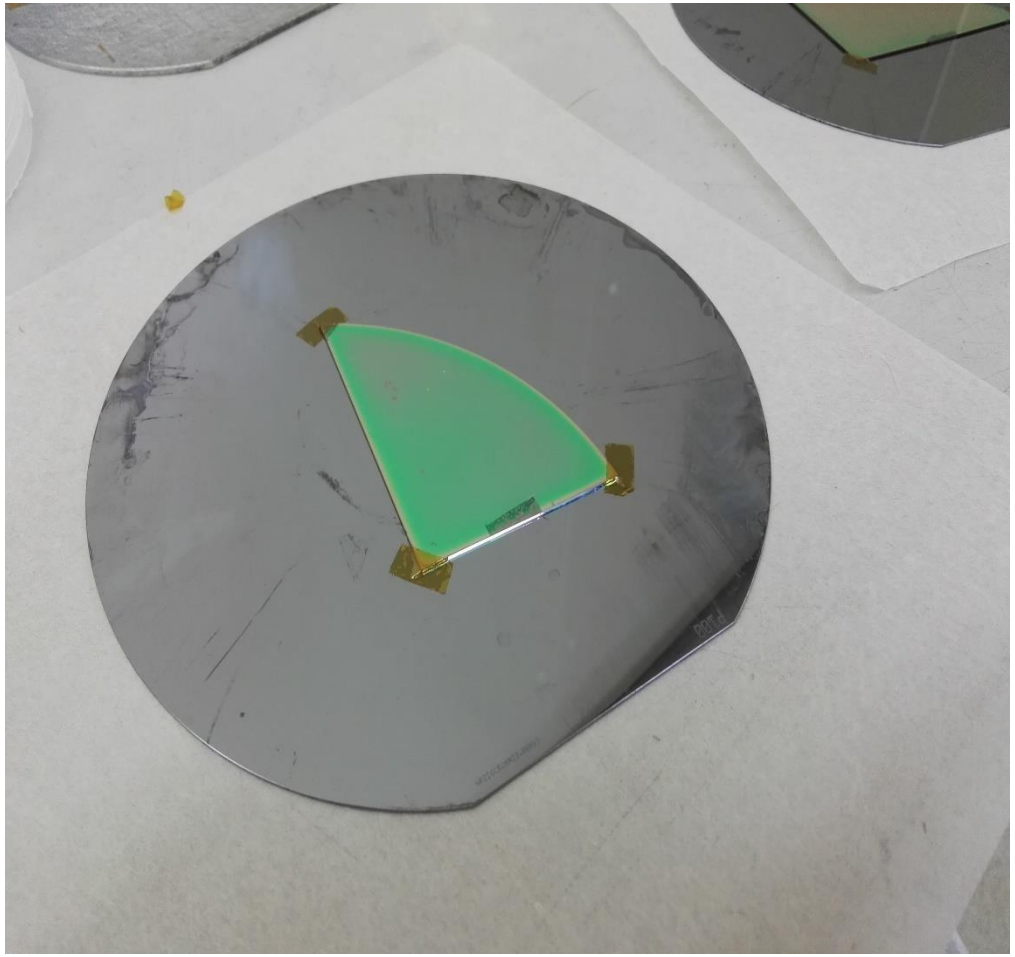
5. Si Wet Etching - Pattern Transfer - KOH bath



Time depending process:
Average: 0.3um/min
Silicon Etch Angle: 54.74º

Si Etching general procedure

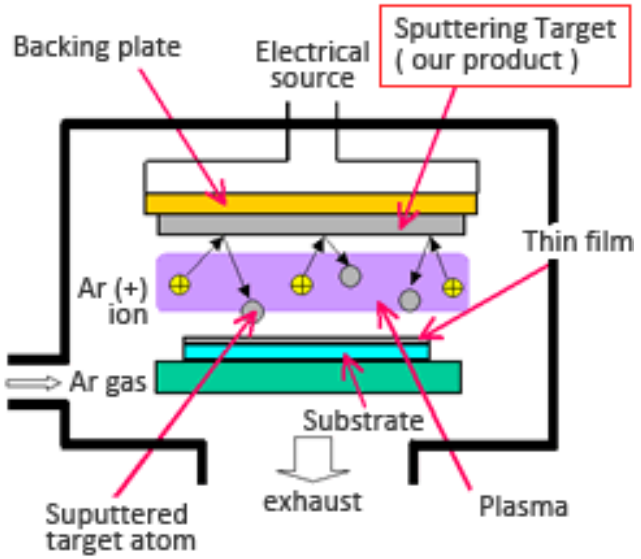
Samples Preparation



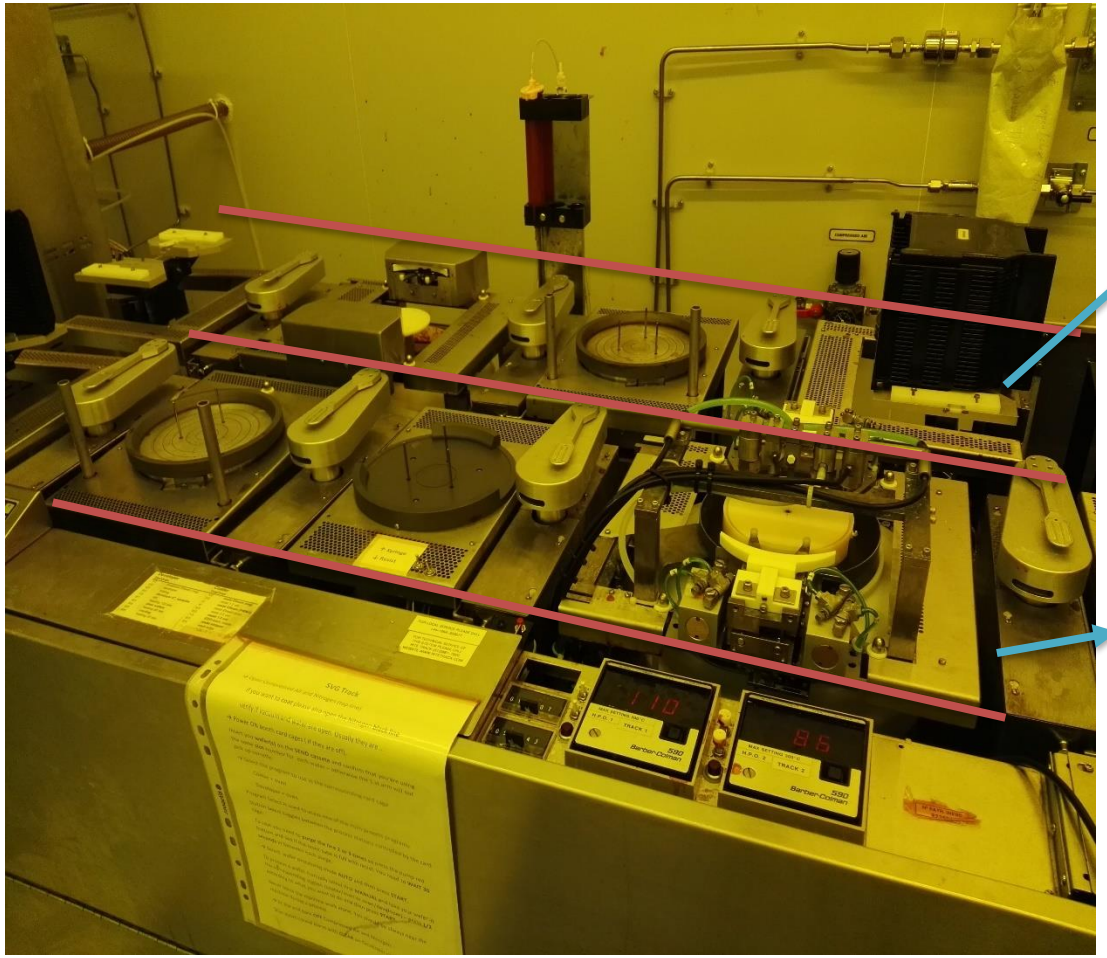
- Parts of 6’ wafer is used for small batch samples testing
- They are attached to 6’ wafer to use on several machines
- Samples are previously coated with 0,3um Cr and 0,5 Si3N4 (Protective coate)

Sputtering Machine Nordiko

- Material deposition on wafer



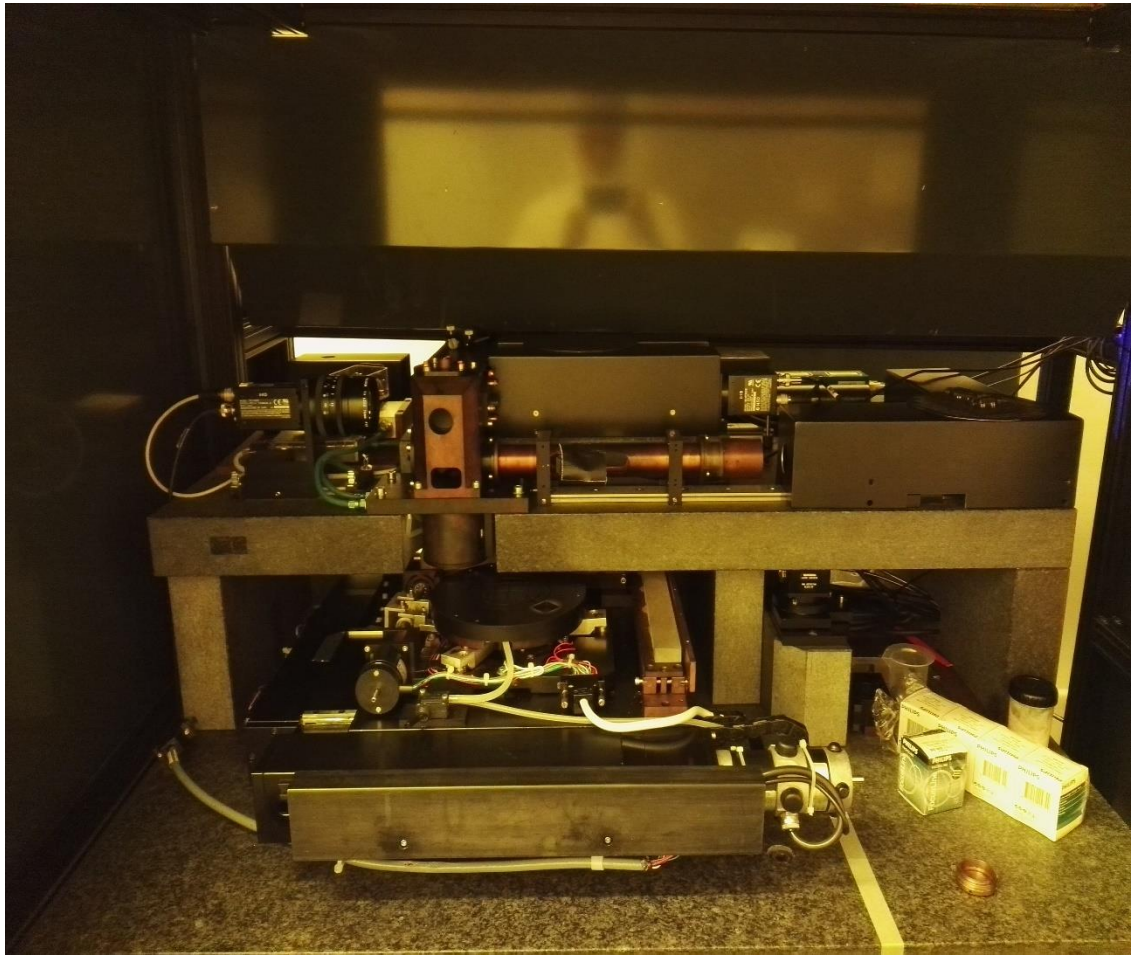
Spin coating and Photoresist cleaning



- Stack of wafers is insert on the machine.
- One by one is automatically applied photoresist by spin coating with an average thickness off 1.5um.

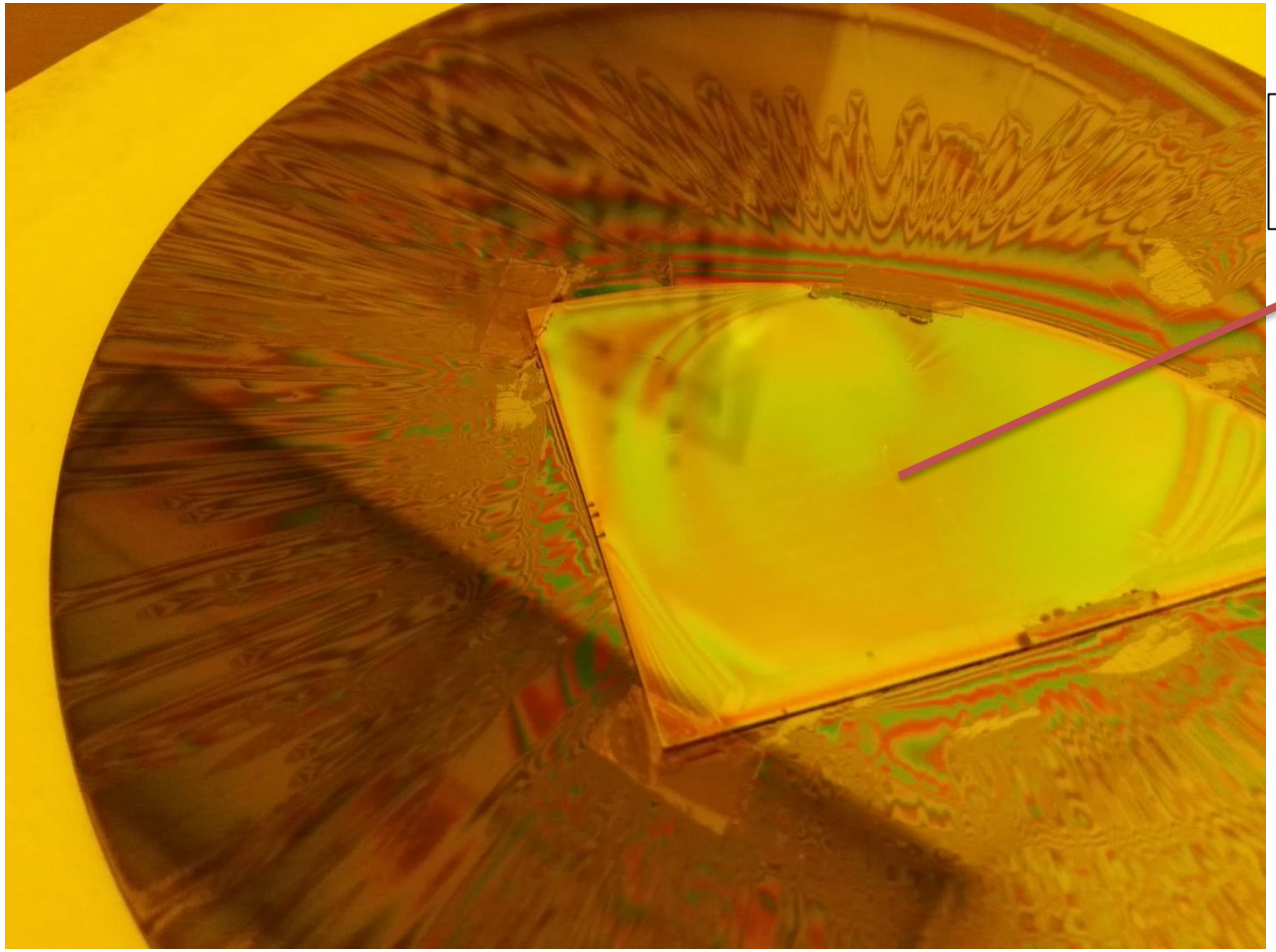
- Stack of wafers is insert on the machine with photoresist to be removed/cleaned.
- Water and acetone bath and spin rinse

Lithography Machine



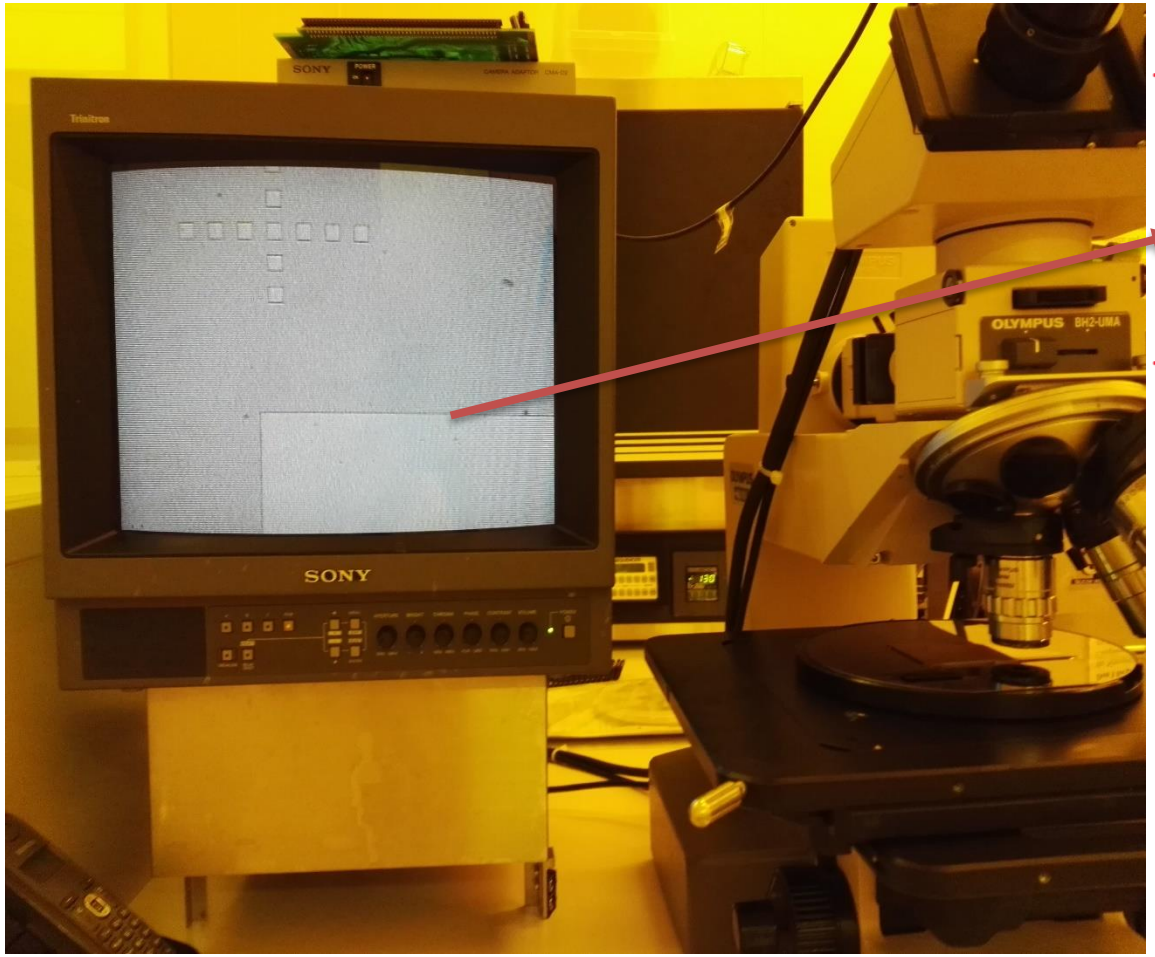
- Lithography machine – high resolution XYZ stages
- Works with positive and negative photoresists.
- “Prints” the 2D pattern on the photoresist for further development.
- e- or e+ are projected against the positive or negative photoresist to soften the photoresist on the exposed area.

Pattern Develop



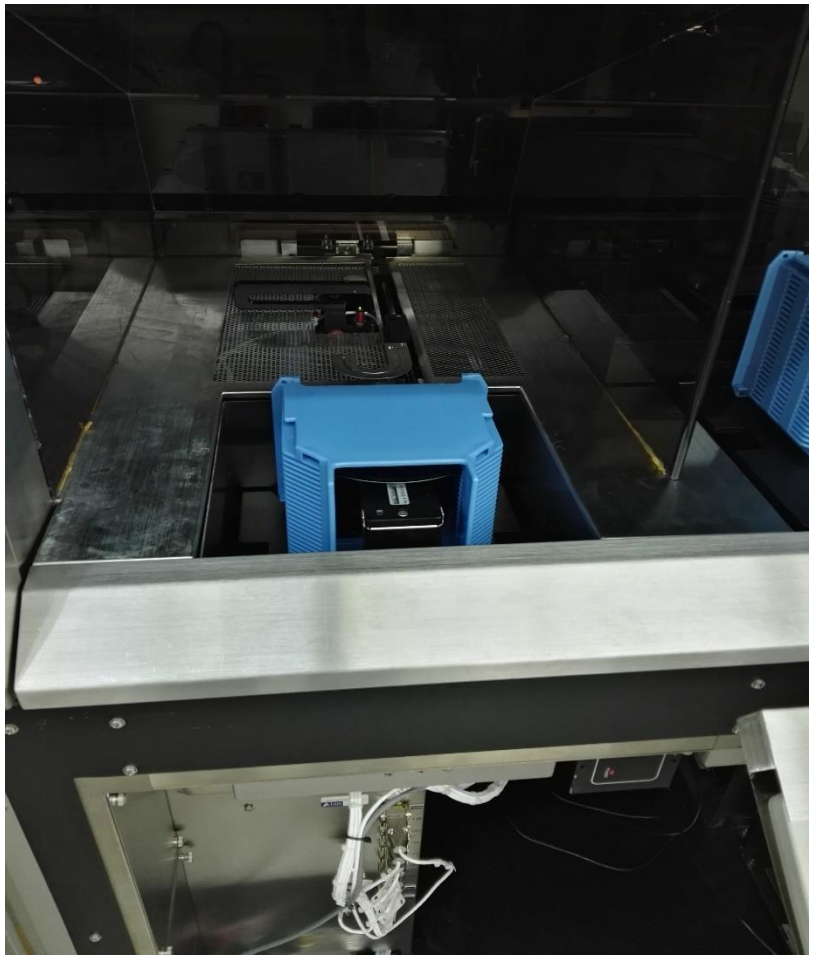
Pattern can be recognizable at naked eye

Patern Develop quality control



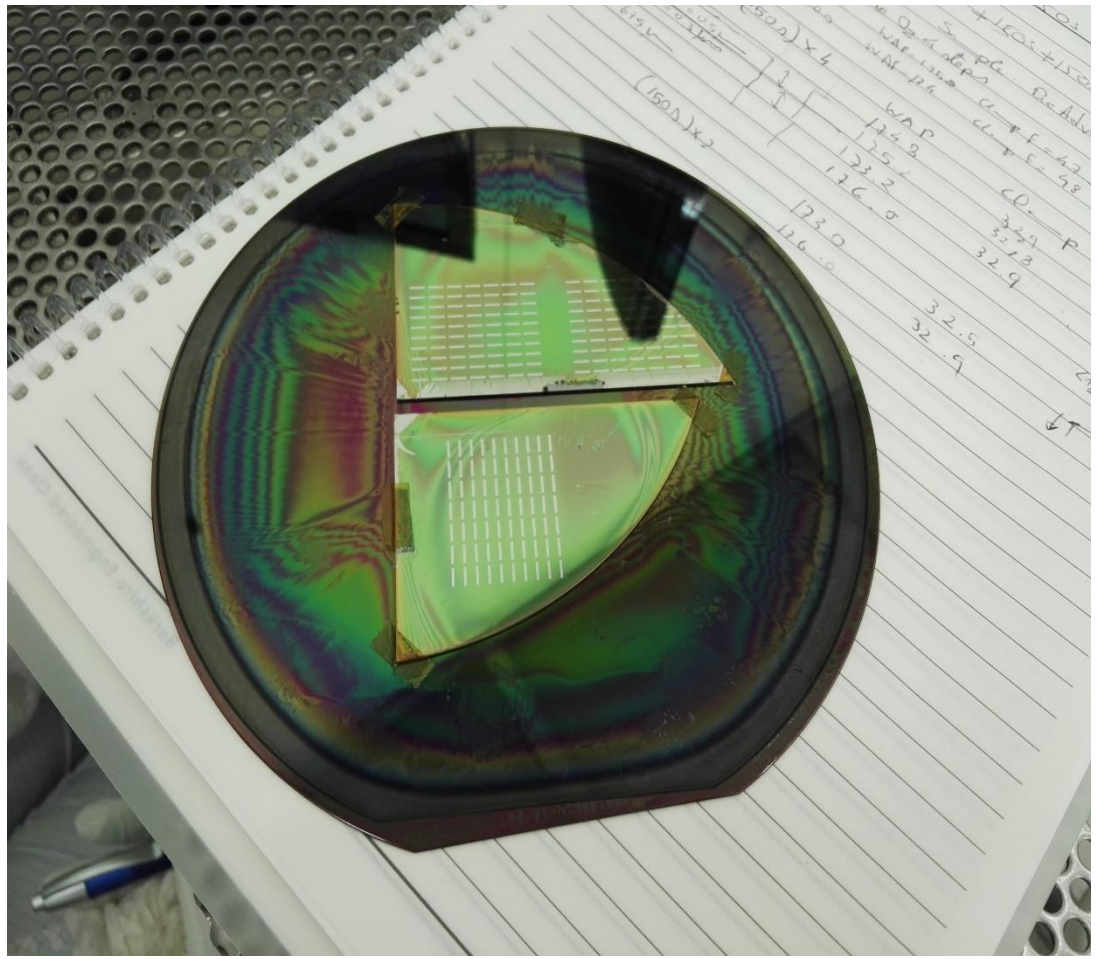
- Check of the entire sample looking for photoresists residues. If it is found any residues, it must go to the cleaning station again.
- In quality control we are looking for the quality of the sharp edges, 90 degree angles, flatness, etc..

LAM machine



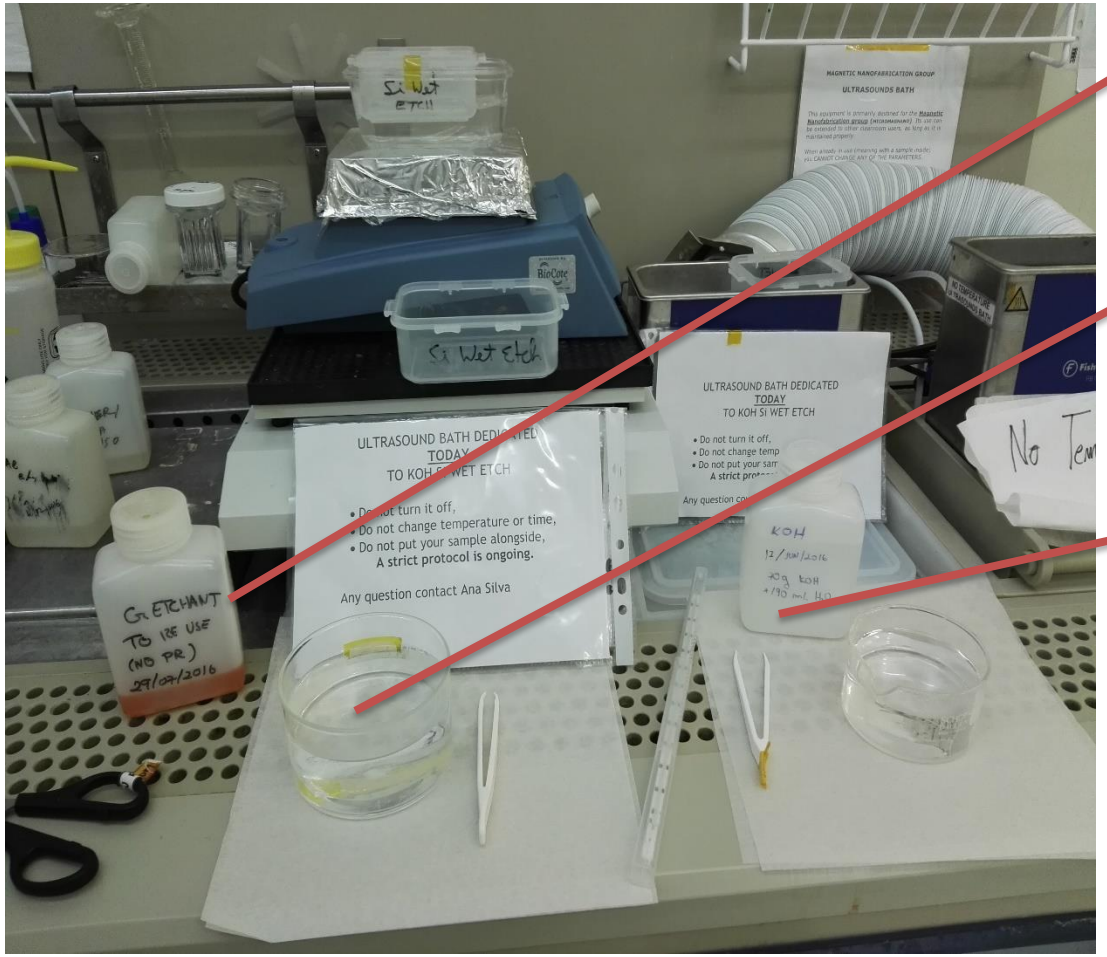
- CF4 gas is used during some minutes to remove the Si3N4 protective layer on the sample.

After LAM



- Sample is cleaned and free of Si3N4.
- Pattern is recognizable and the silver aspect/color on the pattern is the Cr layer.

Setup for Cr remove and Si etching

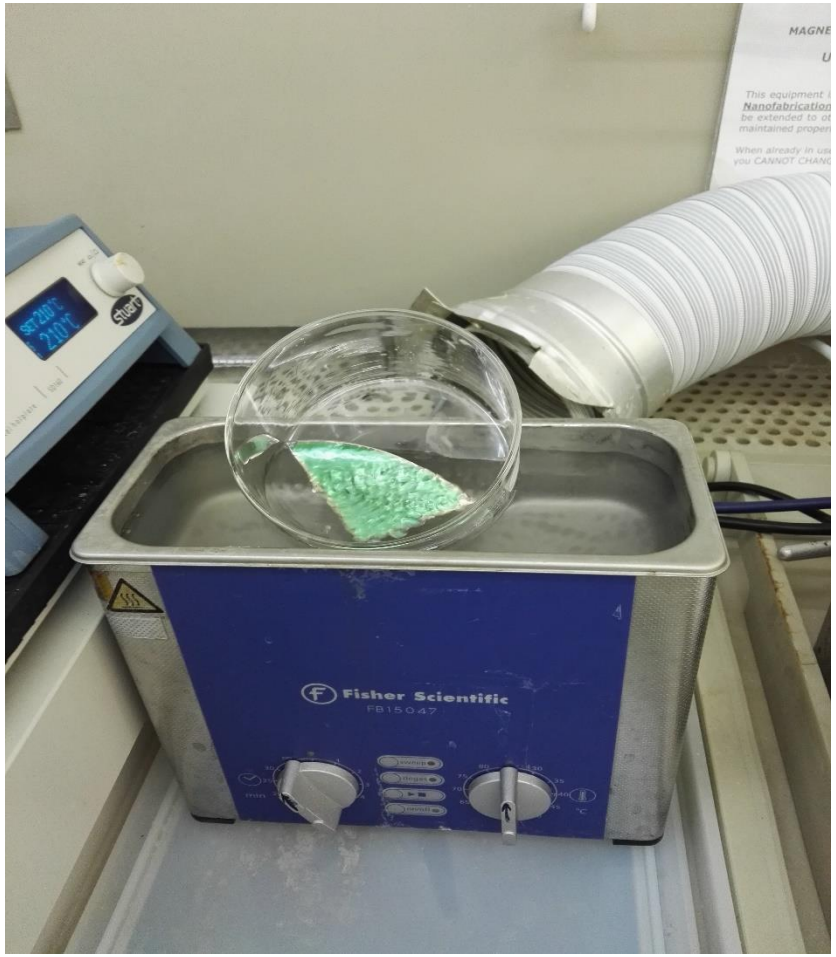


Cr etchant chemical – Not disclosure formula

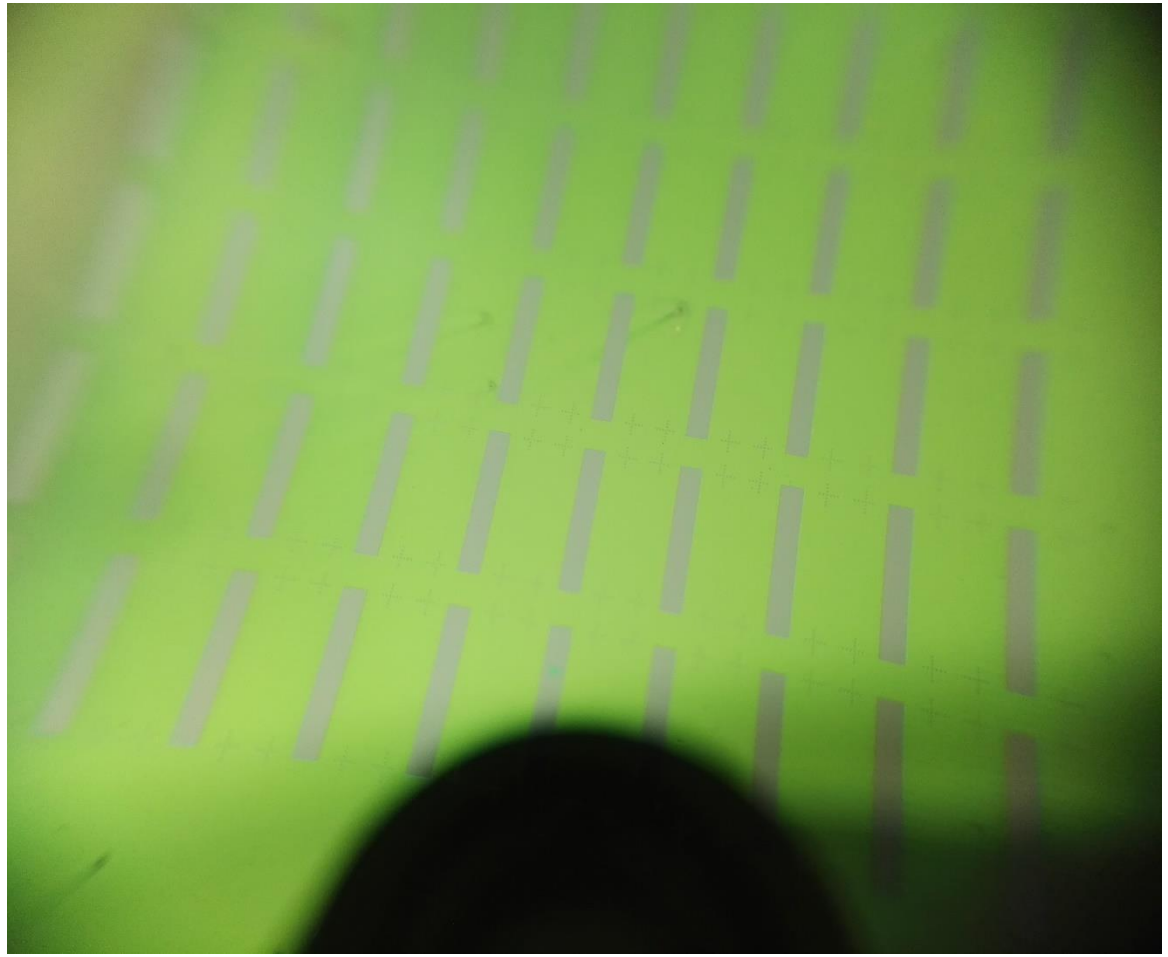
Clean Water

KOH chemical - Silicon etchant

Ultra sound cleaning – IPAN alcohol

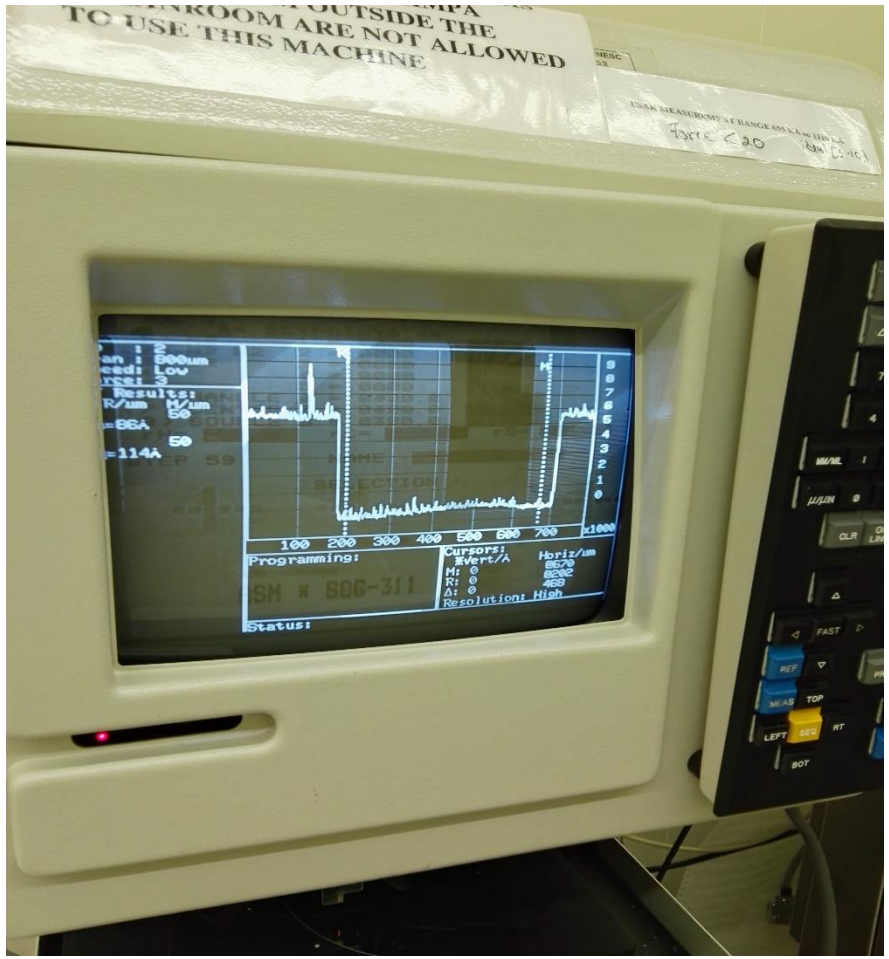


Quality Control: After Cr removal



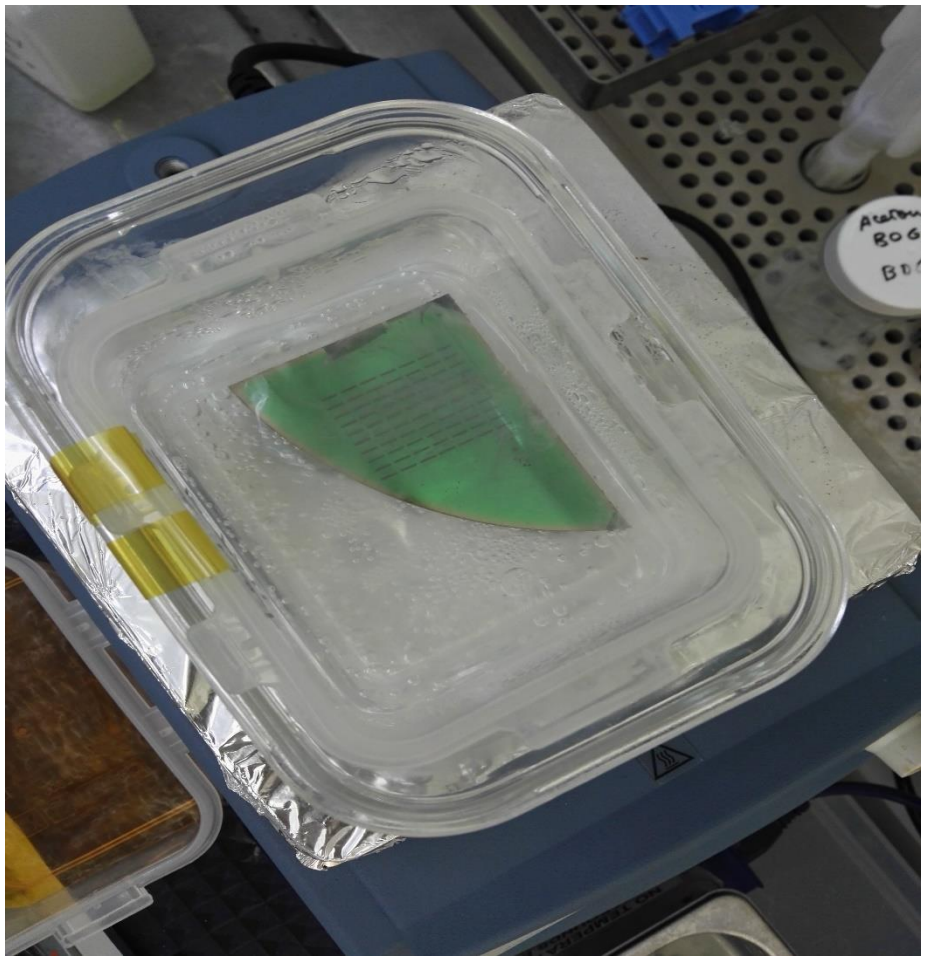
- Green: Si3N4 + Cr
- Silver/grey color : Silicon layer

Quality control: profilometer



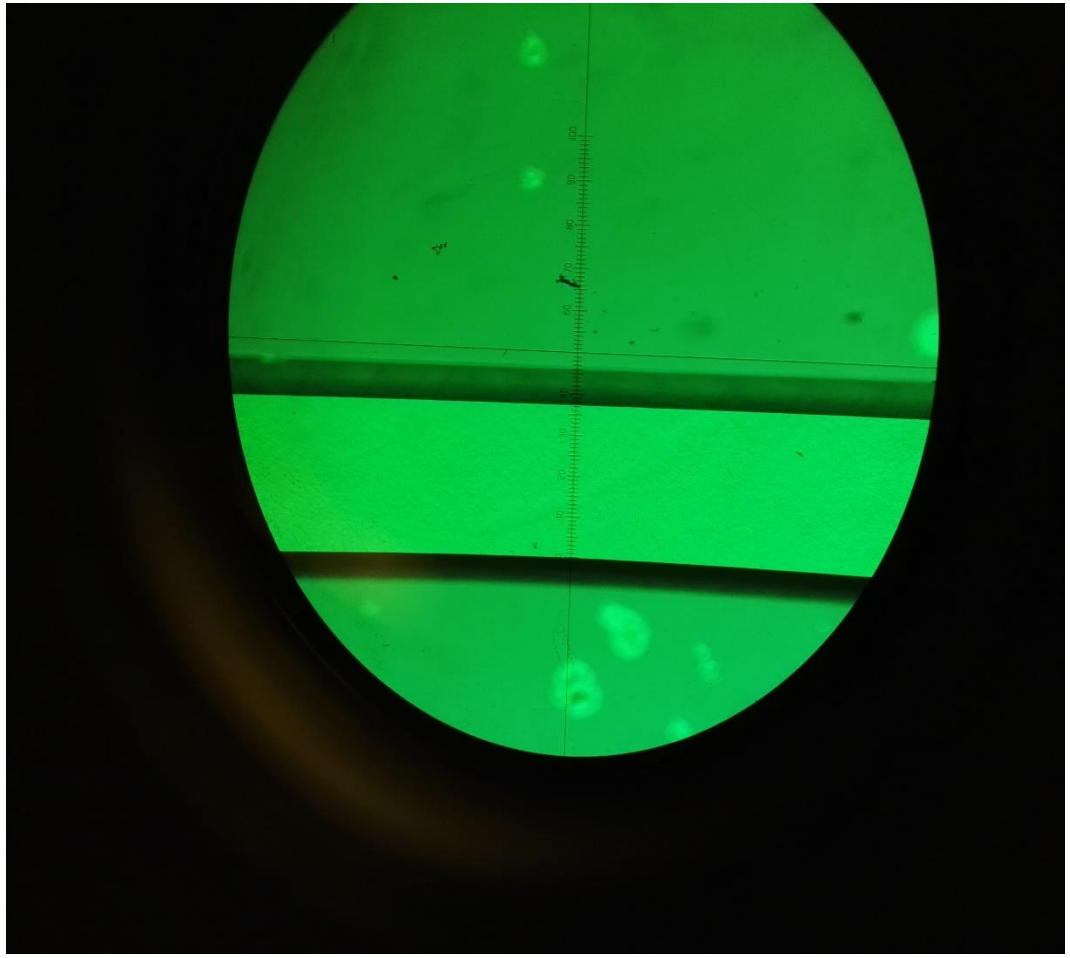
- Profilometer is used to check the height difference between the developed and not developed pattern: It must be similar to the height/thickness of Cr+Si3N4 layer so that it means we are already on the Silicon layer.

Silicon Etching



- Silicon etching – KOH solution - It must be around 65-70ºC and ultra-sound or vibrating plate
- Time dependent procedure: 0,3um/min average speed

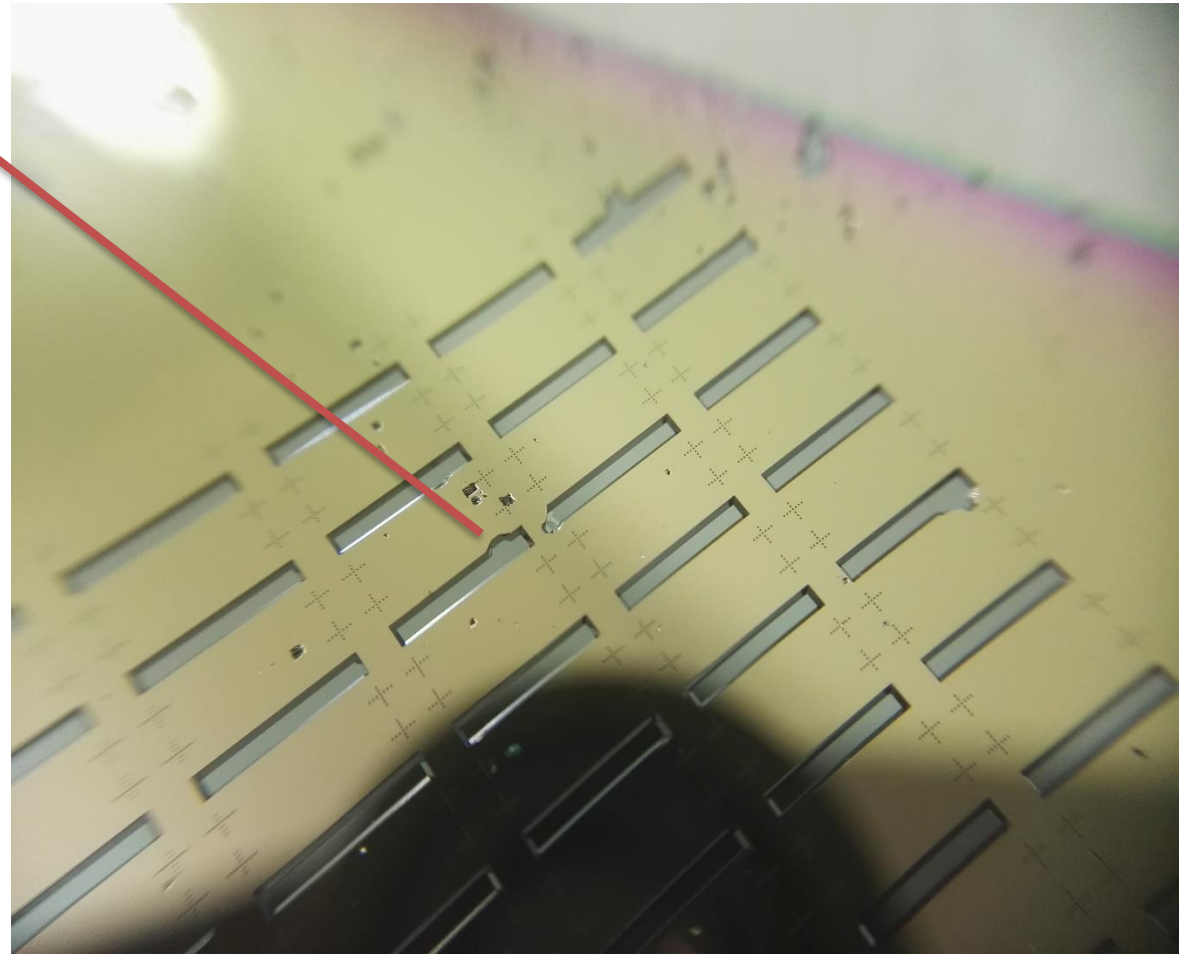
Quality Control: Si Etching



- On the microscope is also possible to measure the V-groove (on this particular geometry) width and estimate how much time remains to achieve the desire width.

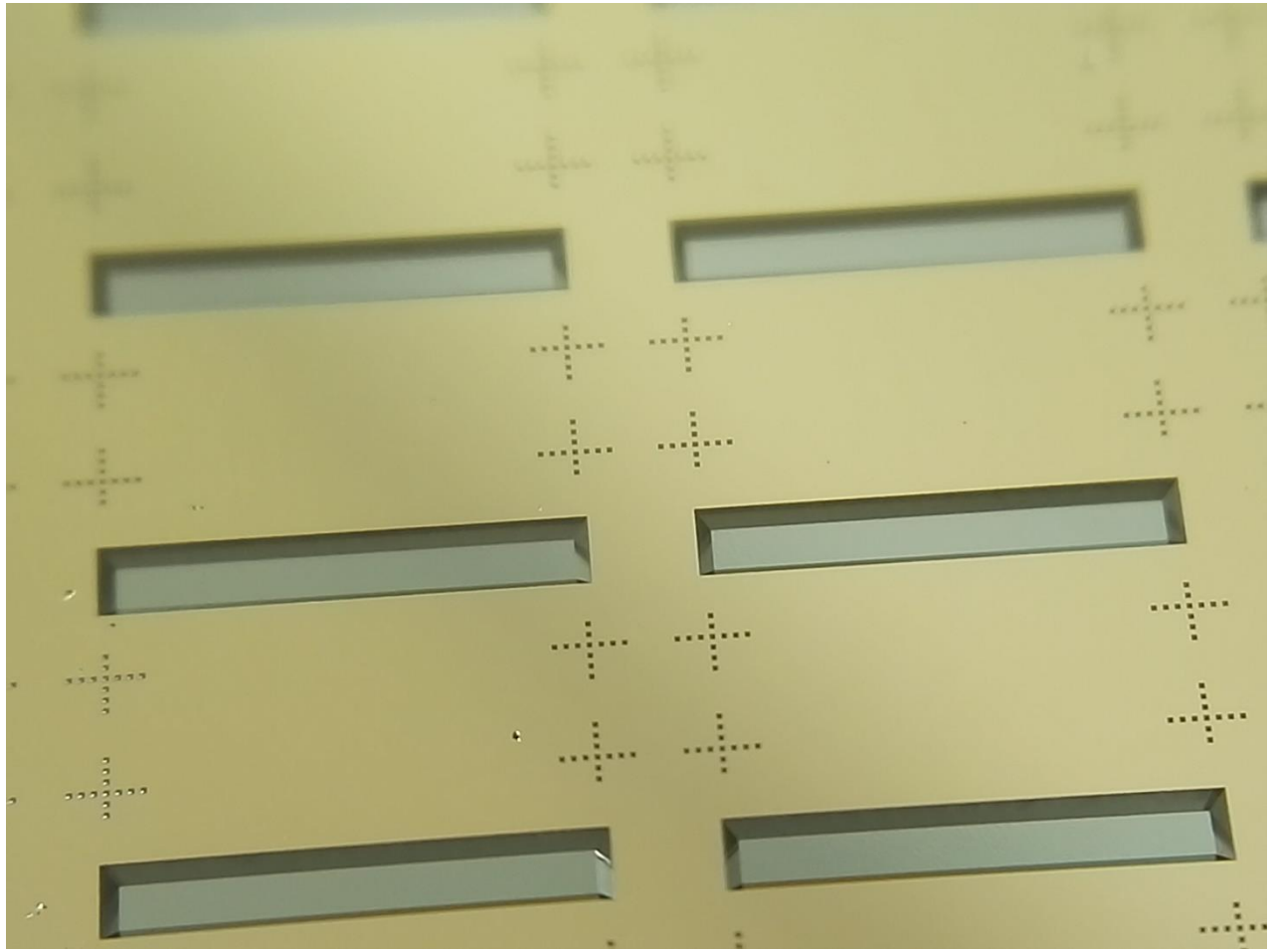
After 6,5 Hours of Si Etching

Mask Collapse: It results on a not protected area of the silicon which means that will be etched by KOH.
It can happen if the initial Cr + Si3N4 layers are not properly deposited.



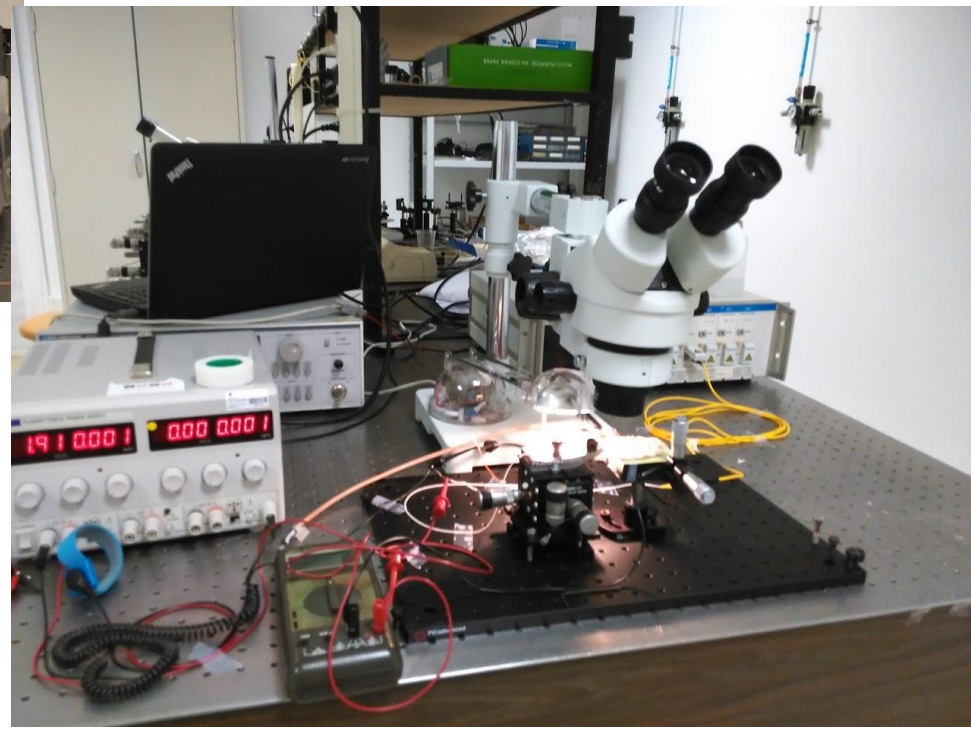
After 6,5 Hours of Si Etching

Well defined cavities and “X” for saw dicing.
500um width and 3mm length and about 130um deep.

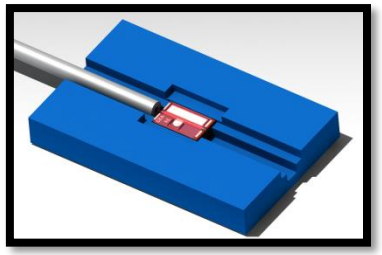


CONTINUING.. LAB TESTING

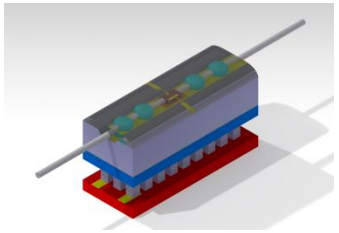
+ Testing



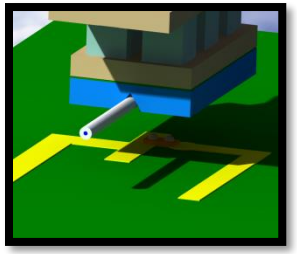
Packaging – generic process



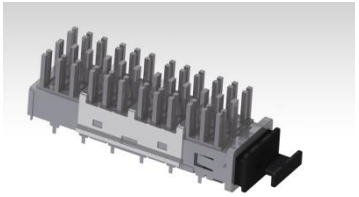
Fiber alignemnt



Gluing and sealing



PCB designd and electro-optic interconnect

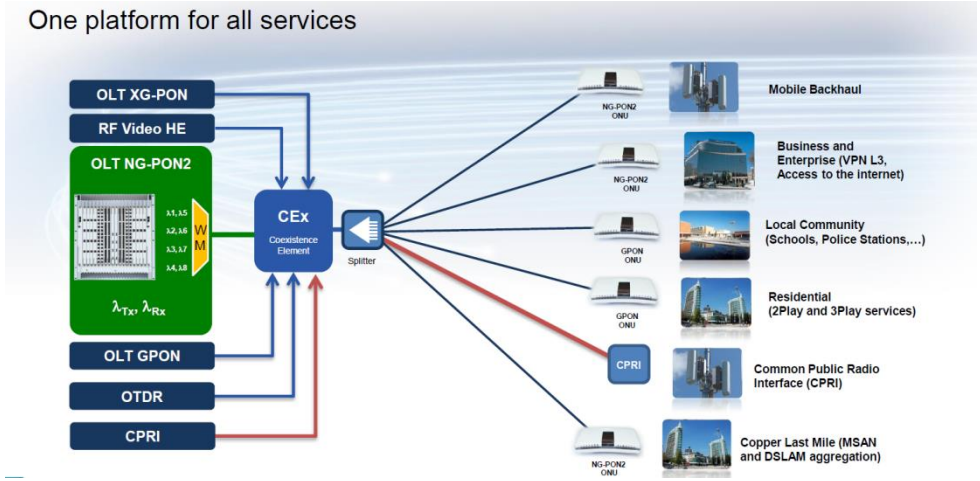


Industry Standard format

Where are we leading to?

FutPON

- Collaborative project with industry
- Funded by P2020



Source: PT Inovação

- Develop the future product line of PT Inovação/Altice in PON technologies
- Opportunity to work from standardization to laboratory and field trials
- Development of PICs for next generation technologies (e.g. NGEPON)

Where are we leading to?

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FutPON

Comparison Between PON Technologies

	Bit Rates Gbit/s		Wavelengths (nm)		Optics	
	DS	US	DS	US		
GPON	2.5	1.25	1490	1310	Fixed Wavelength	
XG-PON	10	2.5	1577	1270	Fixed Wavelength	
XGS-PON (not yet standardized)	10	10	1577	1270	Fixed Wavelength	
NGPON2 (basic)	4*10	4*2.5	1596.34 1597.19 1598.04 1598.89	1532.68 1533.47 1534.25 1535.04	Fixed or Tunable Wavelength	Could go till 8 wavelengths
	4*10	4*10				
EPON	1.25	1.25	1490	1310	Fixed Wavelength	
10GEPON	10	1.25	1577	1310	Fixed Wavelength	
	10	10	1577	1270	Fixed Wavelength	

Source: PT Inovação

Startup collaborating with IT/UA – www.picadvanced.com

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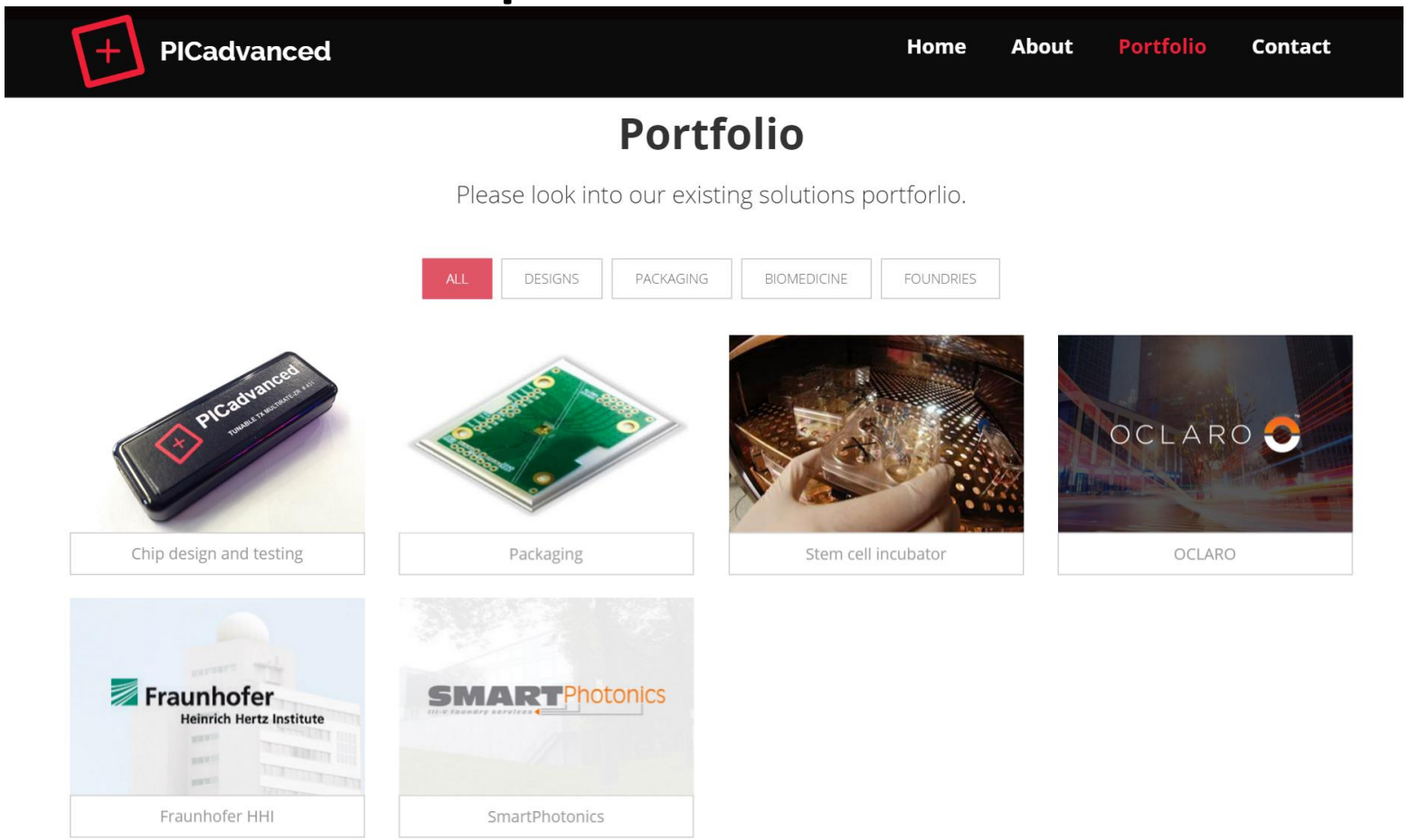

How do we plan to approach the cost reduction?

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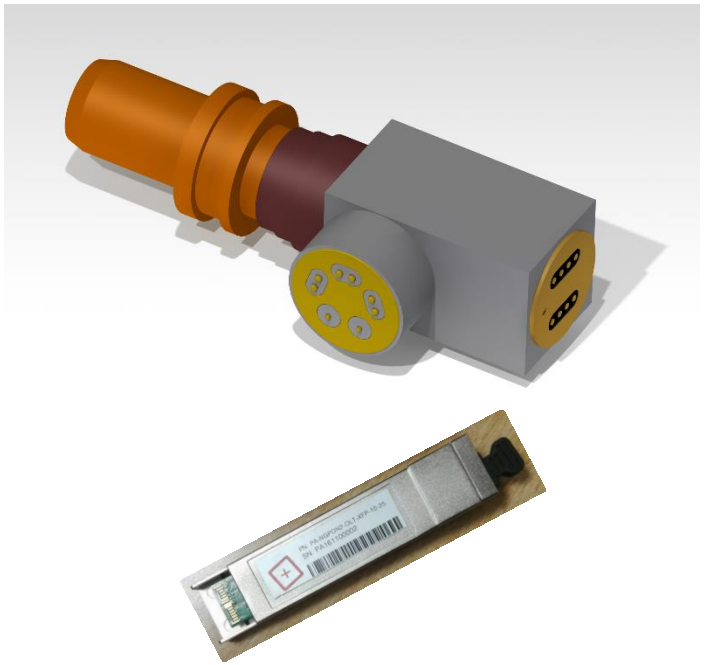
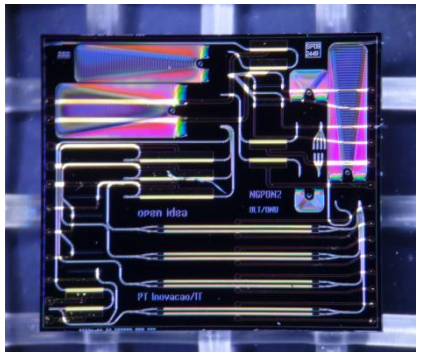
BOSA



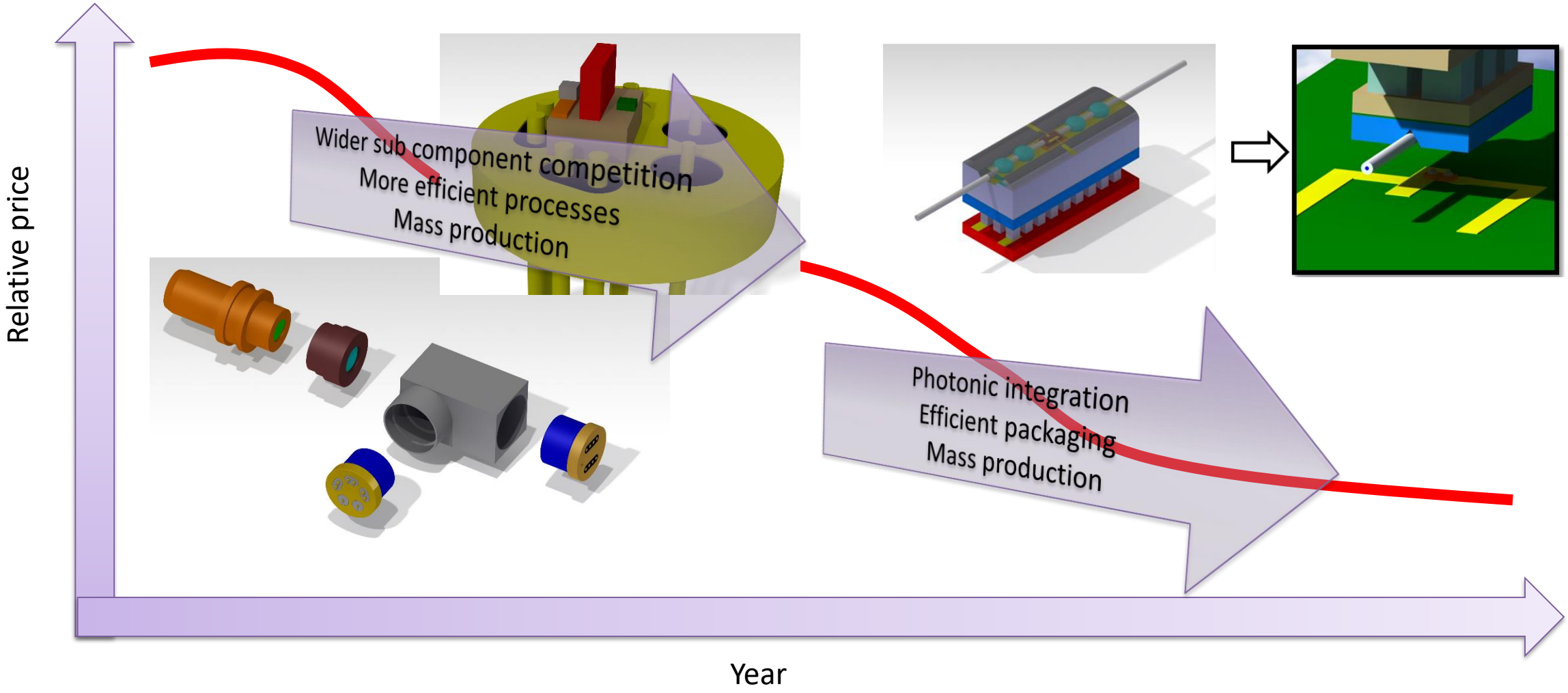
- Alive from 2014
- “typical” approach
- Continuity - Ready for mass production

PIC

- expected 2018 (concepts demonstrated 2015)
- Non-conventional approach
- Potential disruption



The ultimate spark for NG-PON2



TRENDS

Where are we leading to?

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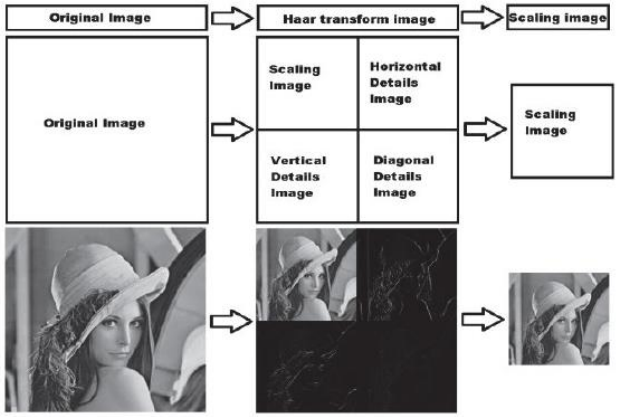
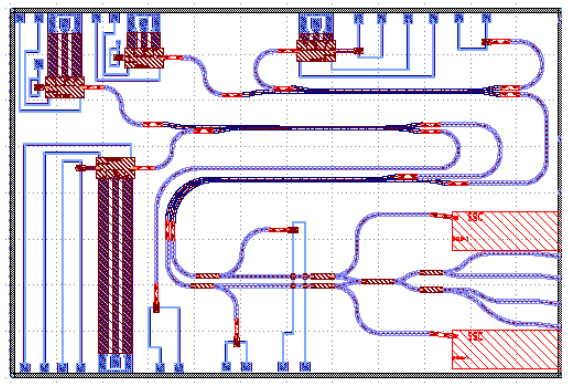
Compress

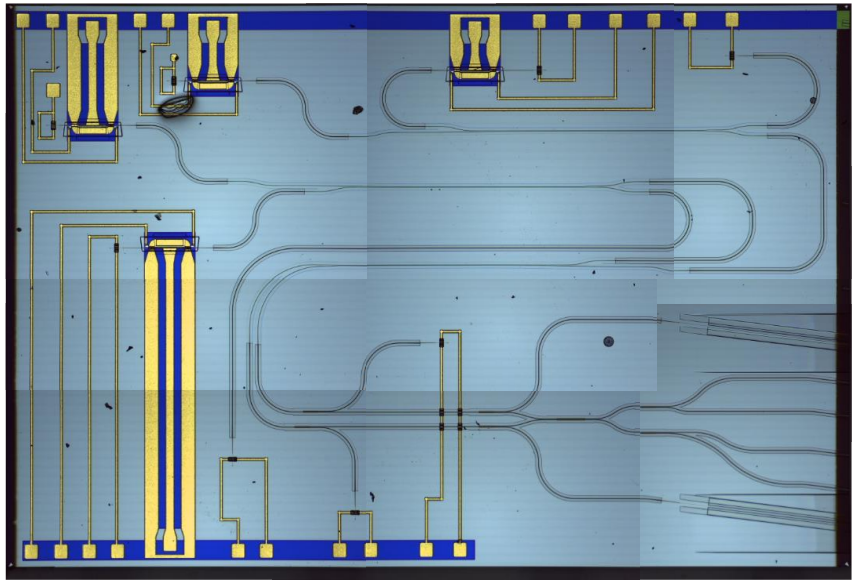
- Scientific project
- Funded by FCT





All-optical line rate, energy aware image De/compression!

- Characterization of existing chips from PARADIGM award
- Development of novel PIC building blocks in colaboration with foundries
- First PIC based all-optical image pre-processor



Think outside the box, with us!

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- Aveiro, Portugal

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CENTRO 2020

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